108 and 124 GHz Fundamental VCOs with 21% and 7% DC-to-RF Efficiency in 22nm CMOS FDSOI

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Abstract — This paper presents the design of two high efficiency fundamental voltage controlled oscillators (VCO) for sub-THz applications. The design optimizes the transistor for voltage gain, swing and PAE at the operating frequency to achieve 21% and 7% DC-to-RF efficiencies. The varactor and back-gate voltages are utilized for tuning control. The back-gate controls improves the relative tuning range of the VCOs by $\sim 50\%$. Layout techniques are employed in the transistor and inductor to improve the VCO frequency. The two VCOs are implemented in 22nm CMOS FDSOI, oscillate at 108.7 GHz and 124 GHz having an output power of 3.41 and -1.45 dBm with a tuning range of 3.4% and 3.7%, respectively. The chip operates at a supply voltage of 0.7V and an I_{BIAS} of 1.4mA with a core power consumption of 10.2mW and 9.9mW, respectively. The active area is 0.095x0.087 mm^2.

Keywords — VCO, CMOS, FDSOI, W-Band, D-Band.

Fig. 1. VCO1 and VCO2 schematic diagram.

I. INTRODUCTION

The advancements in CMOS technology over the past several decades in millimeter and teraherz (THz) frequencies is gaining interest due to the promising applications in the fields of medical imaging, spectroscopy and radar equipment. Such systems are expected to deliver high output power and wide bandwidth operation while consuming low power.

Oscillator is often the "power-hungry" circuit block, and requires improvement in efficiency. Designing a sub-THz VCO with high power and wide tuning range is very challenging. Several studies have been carried out to address it. In [1] and [2] a systematical approach is presented to optimize the available power of a single transistor regardless of circuit architecture by deriving its activity condition. In [3], the fundamental VCO effectively manipulates the dc current of the drain to minimize the ON time of the transistor, while maintaining the same fundamental generated power. Whereas in [4], A single-transistor active feedback network is used to provide the optimum signal swing condition at the gate of the core transistor for maximum PAE.

In this work, we utilize the fundamental VCO topology [3], [5], [6] and utilized the systematic approach addressed in [1] and [2] alongside maximizing PAE of a single transistor[4]. The designed fundamental VCOs achieved a high DC-to-RF efficiency above 100 GHz. These VCOs present a high output power, low voltage and moderate power consumption suitable for W-Band and D-Band medical imaging applications. The narrow tuning range is enhanced with back-gate controls. The transistor core is dimensioned to maximize PAE, voltage swing and optimum voltage ga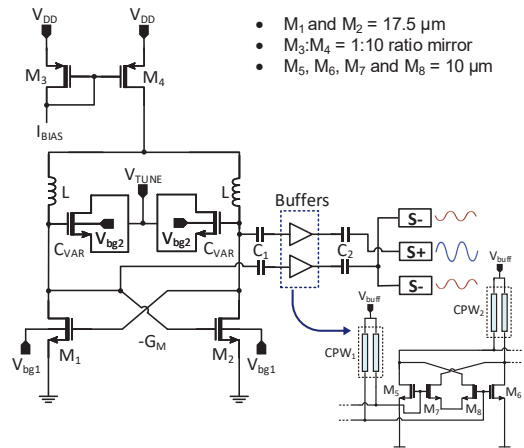in A_{opt}. The Q factor of the inductor is improved with metal fill optimization techniques. The operating frequency of the VCO is increased by careful reduction in parasitic capacitances C_{par} of the transistor and the inductor.

II. VCO DESIGN AND IMPLEMENTATION

A. VCO Core

The VCO core follows a conventional cross coupled pair topology as shown in Fig. 1. The VCO core is composed of G_M transistors, varactors, and an inductor. Two targetted VCOs, namely VCO1 and VCO2 are designed using the same design iteration but with different layout implementations to improve the frequency. The VCO core is crucial in this design. The M_1 and M_2 transistors are sized to 17.5 μm to provide a large voltage swing and a better negative resistance R_{neg} to compensate for the LC tank losses. The M_3 and M_4 form 1:10 current mirrors that offer current bias control for the VCO core. The inductors and the varactors are dimensioned carefully taking the Q factor of the LC tank into account.

B. Output Power Considerations

To achieve high power from a device, the voltage gain from a transistor at designed frequency should be close to unity or greater with a high voltage swing across the transistor [1]. Moreover, at high frequencies the phase shift from gate to drain is not exactly 180° due to parasitics involved. To maximize the output power, the current and voltage phase at the drain terminal should align [2] in the feedback along with
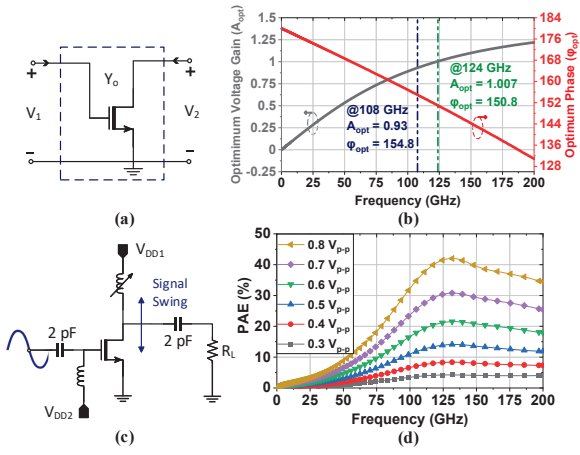
Fig. 2. (a) The two-port network representation of a MOS transistor (b) Simulation of the optimum A and Φ of a stand-alone transistor (c) The setting utilized to obtain maximum PAE for a transistor (d) PAE versus frequency for several voltage amplitudes on the gate from 0.3 to 0.8 V_{p-p}.
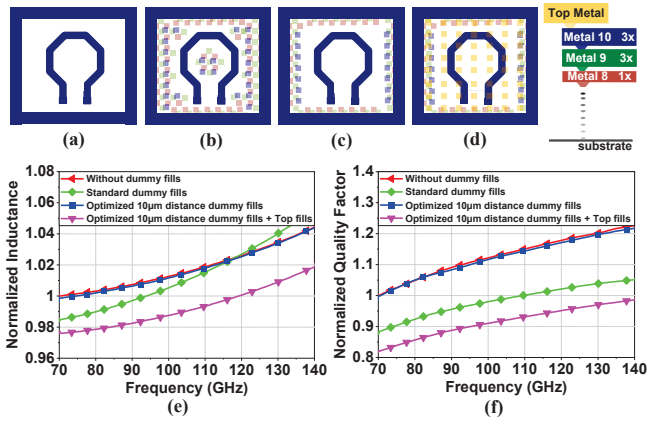

Fig. 3. (a) No dummy fills, (b) Standard dummy fills, (c) Optimized 10μm distance dummy patterns, (d) Optimized 10μm distance dummy patterns+Top Aluminium Fills, (e) Impacts of dummy metal fills on the inductance and (f) Impacts of dummy metal fills on the Quality Factor.
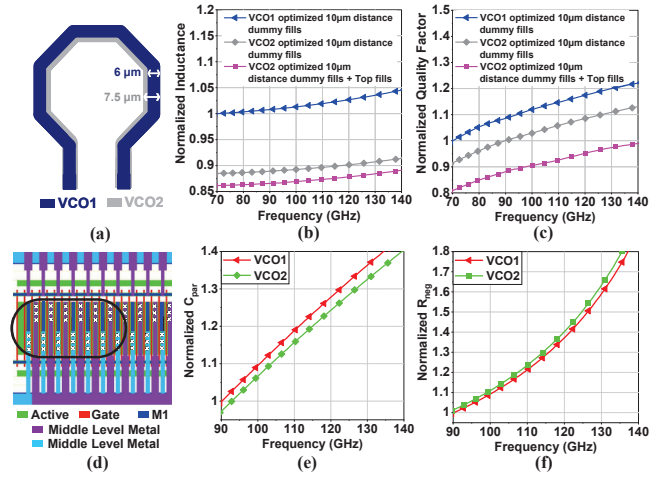

Fig. 4. (a) Inductor width optimization, (b) Variation of inductance over frequency, (c) variation of quality factor over frequency, (d) Transistor layout with circled via connections, (e) Parasitic capacitance C_{par} comparison for both VCOs and (f) Negative resistance R_{neg} comparison for both VCOs.

a unity voltage gain. The two port simulation of the NMOS G_M transistor identifies the A_{opt} and Φ_{opt} for the activity condition [1] as shown in Fig. 2(b). The simulation result depicts that the G_M transistor has an A_{opt} of around unity with phase delay. Furthermore, for a high efficiency oscillator, it is vital to obtain the power added efficiency PAE of a transistor[4]. Key parameters include inductive load, biasing and signal amplitude at the gate. Fig. 2(d) demonstrates the PAE of the optimized G_M transistor over the frequency at different gate signal amplitudes. In this scenario biasing is kept at nominal of 0.8V. The PAE% is observed to increase with the signal amplitudes, and the peak is observed to be around 110-130 GHz with a maximum PAE of 42% for $0.8V_{p-p}$.

C. Q Factor Enhancement with Metal Fill Optimization

Floating dummy patterns are required in submicron CMOS technology to provide the metal density necessary for consistent etching. In the design of high-performance sub-THz VCOs, the LC tank quality is an important consideration. At mm-wave and terahertz frequencies, the varactor's Q factor decreases to single digits, affecting phase noise performance as predicted by the Leeson phase noise model [7]. The Q factor of the inductor is affected by the electromagnetic interaction between the inductor and the fill blocks. The Fig. 3 physical demonstrates the impacts of different dummy fills on inductance and Q factor. The simulation revealed a 3% decrease in inductance and a 14% drop in Q factor due to these fills shown in Fig. 3(c) and (d). To minimize excessive loading of mm-wave signal lines and inductors, the metal density of patterned dummy blocks and metal fillers must be controlled without violating density requirements for the process. The optimized 10μm distance fills shown in Fig. 3(c) without any top or center metal fills in the inductor loop provides a similar performance when compared with no dummy fills.

D. Impacts of Back-Gate Controls

The isolated back-gate in CMOS 22nm FDSOI provides a dynamic control over the threshold voltage V_T. The back-gate can be utilized in the G_M transistors and MOSCAP accumulation mode varactors. In Fig. 1, M_0 and M_1 represent the G_M stage with back-gate V_{bg1} and C_{var} with V_{bg2}. The simulation results revealed that the back-gate can reduce the transistor's negative resistance R_{neg} at the expense of parasitic capacitance C_{par}. For varactor, the back-gate can increase capacitance while decreasing the Q value at specific V_{TUNE}.

E. Matching Buffer

A common source differential buffer with capacitive neutralization feedback is used to match the VCO core to a 50 Ω load. The transistor utilized as capacitor in the feedback provides great reverse isolation and unconditional stability.

F. Frequency Optimization VCO1 vs VCO2

Designing VCO1 and VCO2 for different bands i.e. W and D-band is challenging. The high frequency VCOs are dominated by the parasitics as shown in equation (1) below.
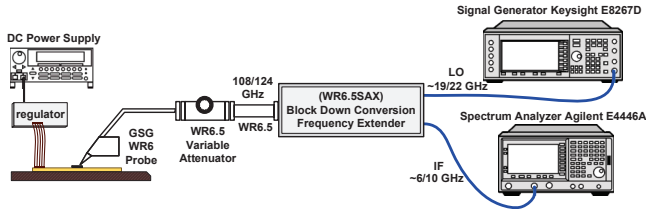
Fig. 5. The block diagram of the measurement setup for both the designed VCO chips.

$$f_{osc} = \frac{1}{2\pi \sqrt{L_T \left(C_{var} + C_{par} + (2C_{buff}) \right)}}, \qquad (1)$$

where for an oscillation frequency f_{osc}, L_T is the total inductance, C_{var} is the varactor capacitance, C_{par} is the parasitic capacitance and C_{buff} is the buffer loaded capacitance, respectively. The layout techniques are critical and these parameters can be optimized to increase the VCO frequency. In VCO1, the inductor dummy fills have been optimized to 10 μm distance as discussed earlier in Fig. 3(e) and (f) to optimize the Q factor and inductance. The G_M transitors utilize parallel gate feed layout to provide better f_{max} and negative resitance R_{neg} when compared with series gate feed and drain over device layout while optimizing the C_{gs} and C_{gd} to target the W-Band frequency. For the VCO2, the layouts of the LC tank's inductor and the negative G_M stage transistors are modified.

Fig. 4(a) and (d) demonstrate the layout optimization performed to improve the VCO frequency. VCO2 inductor width is increased from 6 μm to 7.5 μm that resulted in 12% reduction in the inductance while compromising the Q factor slightly. Unfortunately, top metal fills occurred unintentional in the design of VCO2 as shown in the micrograph in Fig. 6(b) that further reduced the inductance at the expense of affecting the Q factor as shown in Fig. 4(b),(c), and earlier in Fig. 3(d),(e). In VCO2 G_M transistors parasitic capacitance is reduced by reducing the number of connected vias in the source and drain fingers without affecting the current density (μA/μm) thus reducing the C_{par} by 2.7%. These changes resulted in the design of VCO2 with increased frequency performance with drawbacks mentioned in the next section.

III. MEASUREMENT SETUP AND EXPERIMENTAL RESULTS

The 108 and 124 GHz VCOs have been fabricated in 22nm FDSOI CMOS process occupying a chip area of 332x427 μm^2 and the core area of only 87x95 μm^2. The microphotograph of the chip is shown in Fig. 6. The frequency spectrum measurement setups of VCOs are shown in Fig. 5, which consists of WR6 GSG probe, and a WR6.5 waveguide attenuator, to avoid saturation of the spectrum analyzer extension (SAX) module. The SAX module acts as a block down conversion mixer. High side LO 6x(19 and 22 GHz from RF signal generator) is mixed with the probed VCO signal for VCO1 and VCO2, respectively. The downconverted signal is measured with the spectrum analyzer.
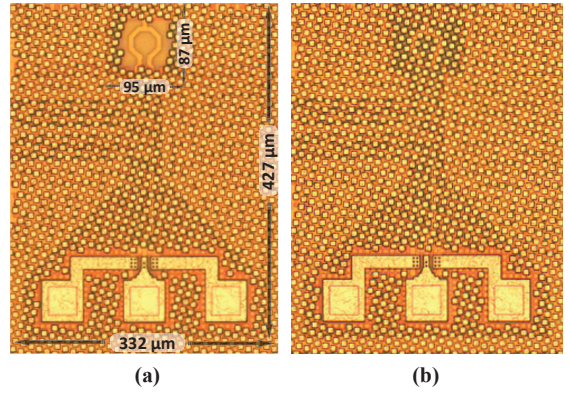

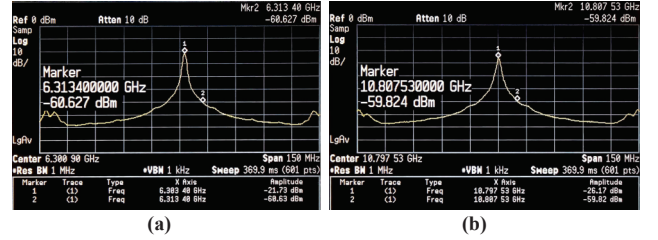Fig. 6. The micro-graph of the oscillator chip (a) VCO1 and (b) VCO2.

Fig. 7. Measured output spectrum of (a) VCO1 and (b) VCO2 after down conversion.

The designed VCO is measured with a supply voltage V_{DD} of 0.7V, I_{BIAS} of 1.4 mA and a V_{TUNE} from 0 to 1V, the core DC power consumption is 10.2 mW for VCO1 and 9.9 mW for VCO2. Both buffers consumes a DC power of 11.5 mW with V_{buff} of 0.8V. Measured phase noise spectra of VCO1 and VCO2 are shown in Fig. 7(a) and (b), respectively. The output power of the VCO can be determined by de embedding losses from the GSG Probe, waveguide, attenuator, SAX module and the cable connecting the spectrum analyzer. The measured output powers are 3.4 dBm for the VCO1 and -1.5 dBm for VCO2 at the center frequencies. Fig. 8(a) and (b) show the measured tuning range of the VCOs from 107.46 GHz to 110.12 GHz and 122.64 GHz to 125.65 GHz for VCO1 and VCO2, respectively. With the back-gate controls, the tuning range improves from 2.45 to 3.39% for VCO1 and 2.42 to 3.65% for VCO2 as depicted in Fig. 9 and 10 with minor effect on phase noise. The DC-to-RF efficiency of the VCO1 and VCO2 is observed to be 21.5% for VCO1 and 7.2% for VCO2, respectively. The phase noise is measured at 10 MHz offset over the tuning range for both VCOs and the results can be seen in Fig. 8(d). VCO2 achieved a higher frequency with slight degradation in phase noise and DC-to-RF efficiency when compared with VCO1 due to higher frequency and lower Q factor discussed earlier. Table. 1 summarises the reported CMOS VCOs in W-Band and D-Band. This work exhibits an excellent output power with high DC-to-RF efficiency.

IV. CONCLUSION

In this work, we presented the design of two fundamental W-band and D-band VCOs utilizing 22nm CMOS FDSOI technology. The VCOs utilize a fundamental architecture to

Table 1. Performance comparison of CMOS VCOs with oscillation frequencies in W-Band (75-110 GHz) and D-Band (110-175 GHz).

| Ref	CMOS Tech.	BW (GHz)	f_{cen} (GHz)	FTR (%)	P_{out} (dBm)	DC-to-RF Efficiency(%)	P_{DC} (mW)	PN [dBc/Hz]	V_{DD} (V)	FOM [8]	$FOM_{(PE)}$ [9]	Area (mm^2)
VCO1*	22nm	106.9-110.6	108.7	3.39	3.41	21.5, 10.12[†]	10.1	-98.9@10MHz	0.7	-169, -166[†]	-176, -170[†]	0.33x0.42
VCO2*	22nm	121.8-126.3	124	3.65	-1.45	7.19, 3.33[†]	9.9	-93.65@10Mhz	0.7	-165, -162[†]	-164, -157[†]	0.33x0.42
RFIC[5]	65nm	114-122	118.3	7.80	-21.5	0.12	5.6	-83.9@1MHz	1	-176	-145	0.58x0.37
RFIC[5]	65nm	-	122.5	4.40	-16.5	1.11	2	-83@1MHz	0.8	-181	-158	0.58x0.37
EuMIC[8]	65nm	113.6-118.8	115	4.40	-2.50	9.07[†]	6.2[†]	-85.3@1MHz	1.2	-178[†]	-178[†]	0.55x0.39
RFIC[10]	65nm	100-110	105	9.5	4.5	5.2	54	-92.83@1MHz	1.2	-176	-187	0.57x0.40
LSSC[3]	130nm	-	91	0.5	4.5	6.12	9.9	-87@1MHz	1.8	-169	-155	0.74x0.68
LMWC[6]	65nm	-	94.6	5.60	-4	2.84	14	-106@10MHz	1.5	-174	-169	0.64x0.38

* This Work, † Core+buffer power consumption
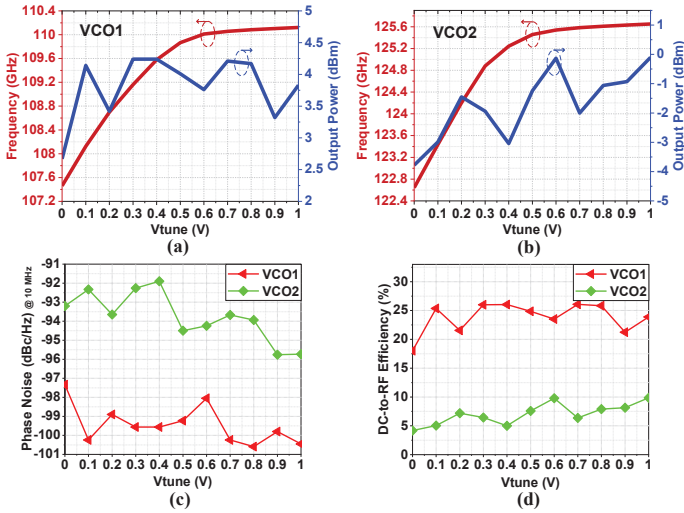
Fig. 8. Both VCOs measured frequency, ouput power, DC-to-RF efficiency and phase noise results over tuning range.
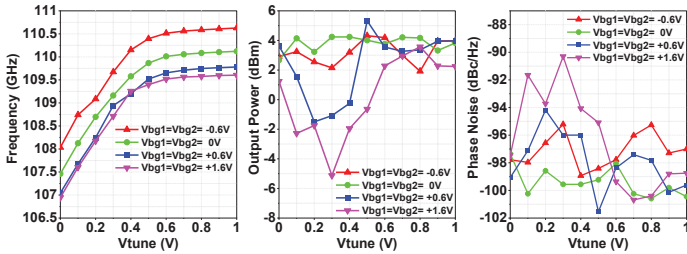

Fig. 9. VCO1 : Impacts of back-gate voltage control on measured frequency, output power and phase noise over tuning range.
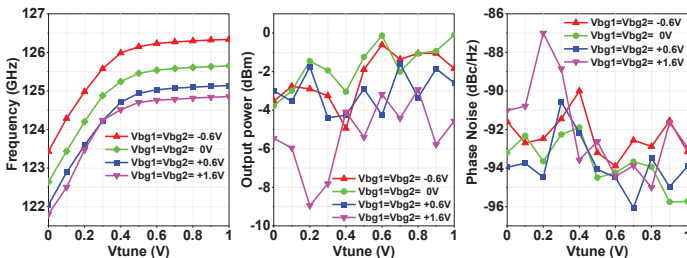

Fig. 10. VCO2 : Impacts of back-gate voltage control on measured frequency, output power and phase noise over tuning range.

demonstrate state-of-the art DC-to-RF efficiencies of 21% and 7% at 108 GHz and 124 GHz respectively. The transistors are optimized to have unity voltage gain, high swing and high PAE at the desired frequency. The tuning range is enhanced by the back-gate controls. The metal dummy fills impacting the Q factor of the LC tank have been optimized. The layout techniques effectively enhanced the operating frequency.

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