A NOVEL DETECTOR MICRO-MODULE FOR COMPUTED TOMOGRAPHY

WU
CHEN

Faculty of Technology,
Department of Electrical Engineering and
Infotech Oulu,
University of Oulu

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Supervised by
Professor Seppo Leppävuori

Reviewed by
Professor Arthur E. Hill
Professor Turkka Tuomi

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Faculty of Technology, Department of Electrical Engineering, Infotech Oulu, University of Oulu, P.O.Box 4500, FIN-90014 University of Oulu, Finland
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Abstract

To realize faster and more precise treatment of patients, CT technology has an urgent demand to make the CT detector arrays larger, and to cover a larger section of the body during one scan of X-ray imaging. A novel detector micro-module is developed in this thesis to meet this demand. In the novel detector micro-module, photocurrent signals are read out from the bottom side of the photodiode array chip. By avoiding the use of the top surface of the chip for routeing, as is the case in conventional CT modules, rectangular detector building blocks containing a certain number of detector elements can be produced. By tiling such building blocks in both x- and y-directions in a plane, detector arrays with any number of detector elements (in multiples of the number in a single building block) can be built. This cannot be achievable by the conventional method.

The novel detector micro-module developed in this thesis consists of an array of 16 × 16 active elements, and the size of the array is $21 \times 21 mm^2$. The array of detector elements is soldered to a multilayer LTCC (low temperature co-fired ceramics) substrate via a BGA (ball grid array) with each element soldered onto one solder sphere, from which photocurrent signals are read out.

In this thesis, the working principle and the evolution of CT detector modules are reviewed and the necessity of developing the novel detector modules is justified. The concept and the structure of the novel detector micro-module are presented. The thermo-mechanical stress modeling and simulation of the structure is performed. The design and the process technology of the photodiode array for the novel detector micro-modules are discussed. The electronic characteristics of the novel detector micro-modules and the related front-end electronics are theoretically analyzed. The LTCC multi-layer substrate is developed. The assembly process of the novel detector micro-module is developed. The basic detector characteristics and light response measurement results of the novel micro-module are presented and discussed.

By improving the photodiode silicon process technology, a dark current density as low as $33 pA/cm^2$ is achieved. Excellent mechanical accuracy is achieved with the LTCC substrate. The dimensional tolerance is +/-10µm and the flatness value is less than 50µm over a distance of a 30.5mm distance. A 64-slice detector module is produced successfully by tiling several novel micro-modules. The novel detector micro-modules are superior to conventional CT modules on many respects while being tileable. Their light sensitivity curve is smoother. They exhibit extremely low signal cross-talk; They have nearly zero wiring capacitance compared to up to 20pF in commercial CT detector modules. They also have almost zero wiring resistance compared to tens of ohm or more than one hundred ohms in the present products.

This result will have a significant impact on CT technology and the CT industry because the detector will be no longer the limiting factor in CT system performance.

Keywords: Computed tomography, detector, detector array, micro-module, silicon

To My Parents

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Oulu, September 2004 Wu Chen

List of symbols, abbreviations and glossary

Latin letters

C	capacitor
C_D	p-n junction diffusion capacitance
C_j	p-n junction depletion region capacitance
C_f	feedback capacitor
CT	computed tomography
C_{ox}	unit area gate oxide capacitance
C_{gsdo}	gate to source and drain overlap capacitance
c	speed of light in vacuum
D_n	electron diffusion coefficient
D_p	hole diffusion coefficient
E_g	energy bandgap
F	frequency
g_m	MOS transistor transconductance
h	Planck’s constant
I	current
I_0	incident light intensity
I_{photo}	photon flux intensity
$I_{leakage}$	photodiode leakage/dark current
J_s	dark current density
K_f	MOS transistor flicker noise coefficient
k	Boltzmann constant
L	channel length of the MOS transistor
L_α	effective absorption length
N_a	acceptor impurity density
N_d	donor impurity density

n_{p0}	electron density in P region at thermal equilibrium
n_i	carrier density in intrinsic silicon
P_{light}	light power intensity
p_{n0}	hole density in N region at thermal equilibrium
p	pitch factor
q	magnitude of electronic charge
R	resistor
$R_\square$	square resistance
R_f	feedback resistor
R_{shunt}	diode shunt resistance
S	light sensitivity
T	temperature
t	time
V	voltage
W	channel width of the MOS transistor
W_d	width of depletion region

Greek Letters

α	optical absorption coefficients
ε	permittivity in vacuum
ε_{Si}	relative permittivity in silicon
η	quantum efficiency
λ	wavelength
θ	projection angle
τ	time constant in electrical circuits
τ_n	N-type minority carrier life time
τ_p	P-type minority carrier life time
υ	frequency of light
μ_i	X-ray absorption coefficient of the ith voxel on X-ray path
ψ_m	PN junction built-in potential

Abbreviations

A/D	analog to digital conversion
ASIC	application-specific circuit
BW	bandwidth
BGA	ball grid array
CDS	correlated double sampling
CMOS	complementary metal oxide semiconductor
CT	computed tomography
CTE	coefficient of thermal expansion
CVD	chemical vapour deposition

DI	de-ionized
DQE	detective quantum efficiency
GE	General Electric
GOS	a ceramic scintillation material, Gd_2O_2S: (Pr, Ce, F)
FET	field effect transistor
IC	integrated circuit
LPCVD	low pressure chemical vapour deposition
LTCC	low temperature co-fired ceramic
MOS	metal oxide semiconductor
NMOS	N-type MOS transistor
P^+	high-doped P region
PCB	printed circuit board
PDA	photodiode array
PMOS	P-type MOS transistor
PMT	photo-multiplier-tube
PSD	power spectral density
SAM	scanning acoustic microscope
SEM	scanning electron microscope
TFT	thin film transistor
UFC	"ultra-fast-ceramic", a ceramic scintillation material
UV	ultra-violet
YGO	a ceramic scintillation material, Y_2O_3-Gd_2O_3: Eu^{3+}

Glossary

Cone-beam: Compared with fan-beam CT, the thickness of the collimator cavity cannot be neglected. The X-ray beam from the source is cone shaped.

Fan-beam: When an X-ray is collimated by a thin slit, the X-ray beam through the collimator forms a fan shape. The thickness of the fan-beam is very small and neglected.

Gantry: A gantry refers to the rotating part (rotating around the patient) of a CT machine. A gantry includes at least the X-Ray source, the detector arc and supporting mechanics.

Helical CT: The same as spiral CT.

Pitch factor: Patient table feed distance counted by the number of detector pitches per 360° rotation; i.e., if the detector pitch is 1mm, if the patient table is fed 1.5mm per 360°, the pitch factor is 1.5.

Projection: A projection is the data set of X-Ray attenuation measurements with the gantry at a fixed angle.

Spiral CT: It refers to the CT system where the patient is fed through a continuously rotating gantry. Thus the focal point of the X-Ray source describes a spiral trajectory relative to patient's body. Refer to Section 1.1.1. It is regarded as synonymous with Helical CT and Volumetric CT.

Voxel: The smallest detection element (pixel) in CT imaging. It can be viewed as a dot in 3-Dimension space. The attenuation coefficient is taken to be the same everywhere inside a voxel.

Z-axis: The direction that the patient table is fed through the gantry is defined as the z-axis direction.

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1 Introduction

1.1 X-ray Computed Tomography

The first functional medical X-ray Computed Tomography (hereinafter CT) system , developed by G. N. Hounsfield in 1972, was for scanning human brain. As a result of his work, the inside of the human body could be imaged non-destructively in 3-dimensions. This greatly enhanced clinical diagnostic ability by precisely and quickly locating the patients' pathological focus and changes. G. N. Hounsfield and A. M. Cormack, who developed the mathematical method for image reconstruction in the first CT system, were awarded the Nobel Prize for medicine in 1979 (Smith & Adhami 1999). Nowadays, X-ray CT has become a routine method in imaging and examining the inside of human bodies in clinical diagnostic practice.

Dramatic developments have been made in X-ray CT technology since Hounsfield's time. Hounsfield's device had only a single detector and it took hours to scan one patient and the image reconstruction process could take over night. In contrast, the state-of-the-art modern CT machine normally contains up to more than 10,000 detector pixels and typically a scan can be completed within the time of a normal breath. Image reconstruction can sometimes be effected on-line (Fuchs *et al.* 2003). Even so, the fundamental principles of image capture and reconstruction remain exactly the same.

In short, X-ray CT builds 3-D images by piling up many slices of the 2-D images of an object one by one. Each 2-D image is a gray-scale picture within which different gray level represents different attenuation magnitudes in the X-ray path. An example of a 2-D slice and the 3-D image is shown in figure 1.1.

More details on X-ray CT working principle are discussed in Chapter 2.

Fig. 1. An X-ray CT image of a human skull; a 2-D slice image (on the left) and the reconstructed 3-D image (on the right).

The CT X-ray detectors, which convert X-ray signals into electrical signals, are key parts of the X-ray CT system in that they are one of the determinative factors for the CT scanning speed, imaging resolution and system dynamic range. They are the subjects of this thesis.

1.2 Purpose of the study

The CT technology, as well as CT industry, has been developed very rapidly, especially after the concept of spiral scanning was introduced in 1990. The market demands CT machines with higher and higher scanning speeds, which in turn requires the incorporation of more and more detector elements into the CT system. However, a bottleneck is set by the X-ray detectors. As will be shown later, the detector modules manufactured with present methodology can only incorporate a limited number of detector elements. Beyond the limit they suffer problems such as too dense a wire-bonding density and other manufacturability problems, high parasitic capacitance, low active area ratio, low production yield and high cost.

This thesis proposes a novel detector micro-module structure that addresses these problems. With the proposed detector micro-module, detector modules with an unlimited number of detector elements can be built.

The micro-module concept, the assembly method, the theoretical analysis of the noise performance, the thermo-mechanical simulation of the structure, and the opto-electrical measurement results of the novel detector micro-module are discussed in this thesis. The results are compared to those of the conventional CT detector modules. The design and manufacturing processes of the key parts of the detector micro-module, i.e., the ultra-low dark current silicon photodiode array and the LTCC substrate, are also presented.

1.3 Contribution

The novel CT detector micro-module described in this thesis was the contribution of the author with the assistance of co-workers. The development work was coordinated by the author. The author designed the novel detector micro-module structure with co-workers. The author also designed the silicon detector structure, detector layout, detector processing parameters, and the principle of the assembly procedure of the detector micro-module. The practical assembly process was developed by the author and the co-workers. The author designed and guided the thermo-mechanical modeling and simulation of the novel micro-module structure. The author also designed and performed the concept verification test procedure of the novel micro-module, participated in the development and validation of the light response measurement setup and the other measurement setups. All the test circuits and PCBs used in the measurements were designed by the author. Most of the measurements and tests in this thesis were performed by the author.

1.4 Contents of the thesis

Chapter 1 gives brief introduction to the subject and the application background of this thesis. In chapter 2, The basic principle of the X-ray CT image reconstruction method and algorithm is presented. The typical setup of a modern CT system is presented. State-of-the-art CT detector modules are discussed in detail. Their structures, manufacturing procedures, key materials and characteristics are discussed. The evolution history of X-ray CT detectors is introduced to conclude the significance of this thesis. The research works carried out by contemporary researchers on the same subject are also reviewed. In chapter 3, the concept of the novel detector micro-module is discussed in detail. The structure is described. The concept of the tileable micro-modules is discussed. The analysis of the corresponding pre-amplification electronics is discussed. The concept verification test results are presented. The main manufacturing steps are discussed. The thermo-mechanical modeling and simulation of the structure are discussed. Chapter 4 covers the design and manufacture of the novel micro-module. The design and process of the silicon photodiode array for the novel detector micro-module are discussed. The photodiode measurement results are also presented. The design and processing of the LTCC substrate are discussed. The assembly processes of the micro-module are also discussed. In Chapter 5, the module-level light response measurement results and other characteristics measurement results are presented. Chapter 6 is the conclusion of this thesis.

2 X-ray Computed Tomography detector modules

This chapter gives the application background and technical background of CT detector modules. A brief introduction of X-ray CT working principle is given. The structure and the working principle of a modern X-ray CT detector module is discussed. The key parts of a CT detector module and their key characteristics are discussed. The evolution history of CT detector modules is reviewed. The predicted future development trends of CT technology and CT detector module technology are presented. At the end of this chapter, the limitation set by the current manufacture approach is discussed. A literature survey on the latest efforts on next-generation solutions is presented.

2.1 X-ray CT systems

2.1.1 X-ray CT working principle

An incident X-ray is attenuated when it passes through an object. The magnitude of the attenuation depends on mainly the X-ray's energy and the material. A material's ability to attenuate X-rays is defined as its attenuation coefficient, which is dependent on the material density.

The 2-D or 3-D X-ray CT images, which reflect the tissue density distribution inside the patients' bodies, are images of the distribution of attenuation coefficients in the volume. The principle of acquiring the distribution of attenuation coefficients is explained briefly as follows.

In an actual CT system, we assume that the path of an X-ray beam through the object being scanned consists of a set of volume elements (voxels). Each voxel has a unique attenuation coefficient. Inside a voxel, the attenuation coefficient can be considered as uniform because a voxel is the smallest volume of interest. It is shown in Fig.2 (UK, CT scanner evaluation center 2002).

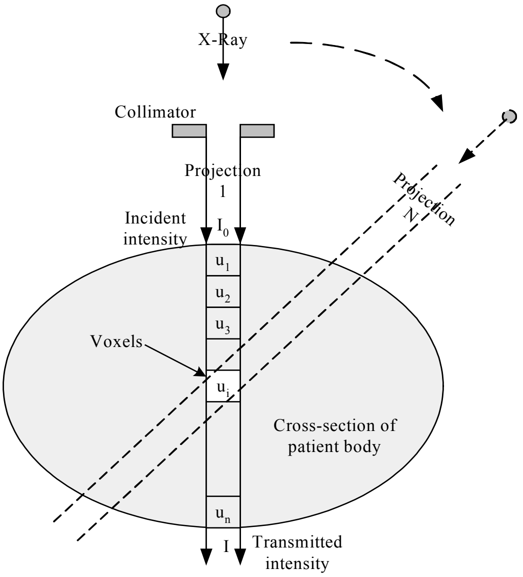


Fig. 2. Distribution of voxels and the corresponding attenuation coefficients on the incident X-ray path.

The X-ray intensity before passing through the patient's body is I_0, and the intensity after passing through is (Cho *et al.* 1993)

$$I = I_0 e^{-(\mu_0+\mu_1+...+\mu_n)x} \tag{2.1}$$

where μ_0, μ_1 ... μ_n is the attenuation coefficient associated with voxel No.0, 1… n; x is the length of each voxel in the X-ray direction.

Solving equation (2.1), we have

$$\mu_0 + \mu_1 + \mu_2 + ... + \mu_n = \frac{1}{x} In(\frac{I_0}{I}) \tag{2.2}$$

If we rotate the projection angle, as shown in Fig.2, to acquire a sufficient number of equations like (2.2), we shall be able to determine every μ_i. Thus we can acquire the 2-D image of one slice of the object. By combining many such slices together, we obtain the 3-D image. This is the fundamental principle of X-ray CT imaging.

The volume of calculation required to solve a linear equation array such as (2.2) is too huge. Instead of that the inverse Randon transform is solved to determine the attenuation distribution (Herman 1980)

$$f(x,y) = -\frac{1}{2\pi^2}\int_0^{\pi}\int_{-\infty}^{+\infty}\frac{1}{t - x\cos\theta - y\sin\theta}\cdot\frac{\partial f(t,\theta)}{\partial t}dtd\theta \tag{2.3}$$

where f(x, y) and f(t, θ) are the attenuation distribution in (x, y) and (*t*, θ) coordinates. (t, θ) is a convenient coordinate for characterizing X-ray projections. In reality, the path with "projection 1" shown in Fig.2 is repeated many times to cover the whole object with an even displacement perpendicular to the projection direction. The displacement of two neighbouring paths is t. Then the projection angle is rotated by θ and the same projection and displacement are repeated. Thus f(t, θ) is the attenuation with a certain projection angle and a certain displacement.

In short, the inverse Randon transform transforms a coordinate convenient in CT projections, into (x, y) coordinates, which is convenient for human minds to recognize.

To avoid the ill-posed problem in the discrete inverse Radon transform, a Filtered Back Project algorithm (2.4) is developed and applied in actual systems. (Herman 1980)

$$f(x,y) = \int_0^{\pi}\left[\int_{-\infty}^{\infty}P_\theta(\omega)|\omega|e^{j2\pi\omega t}d\omega\right]d\theta \tag{2.4}$$

Another thing to keep in mind is that the attenuation coefficient of a material is dependent not only on the material, but also on the X-ray energy. This means that, at one given voxel, the attenuation to incident X-rays from different directions is different. For this reason, a monochrome X-ray source would be desirable. However, monochrome X-ray sources are too expensive for most applications. Correction of this error makes the reconstruction algorithm even more complicated.

2.1.2 Early X-ray CT

The working principle of the very early X-ray CT machines is a straightforward application of the above method. (Kak 1987)

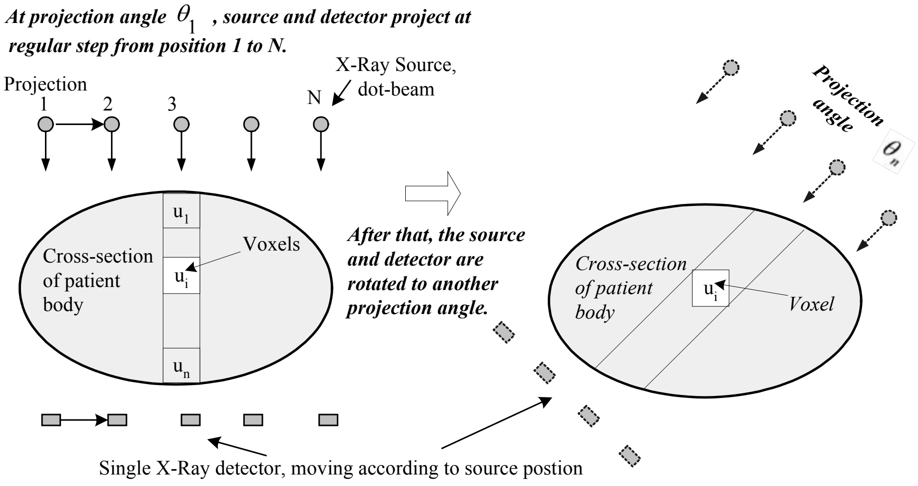


Fig. 3. Working principle of the early X-ray CT system; Left: at one projection angle, the X-ray dot source and the detector move from position 1 to N. Projection data are acquired in regular step, until the full body has been covered; Right: The X-ray dot source and the detector rotate to another projection angle, the process is repeated.

As shown in Fig. 3, the early X-ray CT is composed of a "dot-beam" X-ray source and a single X-ray detector. At one projection angle, the X-ray source moves at a regular interval to acquire a set of parallel projection data. When the whole area of interest has been covered, the X-ray source rotates to another projection angle, and repeats the move at regular intervals to acquire another set of parallel projection data again. This process is repeated until the total rotation angle is 180 degrees, which means that enough data have acquired to reconstruct the 2-D slice image. Then the patient is moved along the Z-axis for one voxel length and the whole process is repeated again to acquire another 2-D slice. Such a system is referred as a "parallel beam system". It takes minutes to finish one rotation, up to hours to acquire the full picture. It is too slow for many applications because the patient has to keep still throughout the scanning in order not to blur the image.

2.1.3 Modern spiral X-ray CT

In 1990, the concept of spiral scanning was introduced (Kalender *et al.* 1990, Crawford 1990). In a spiral scanning X-ray CT, the X-ray beam is limited by a parallel collimator to form a fan-shape. It is thus called a fan-beam X-ray source. The patient is continuously translated through a rotating X-ray fan beam. One or a few rows of detectors are mounted on the opposite side of the X-ray source with the relative displacement from the source kept the same. The detectors measure and record the attenuated X-ray signals at regular projection angles. The patient is fed at a certain speed. Consequently, the X-ray source focal spot describes a “spiral” trajectory relative to the patient. The concept is shown in Fig. 4.

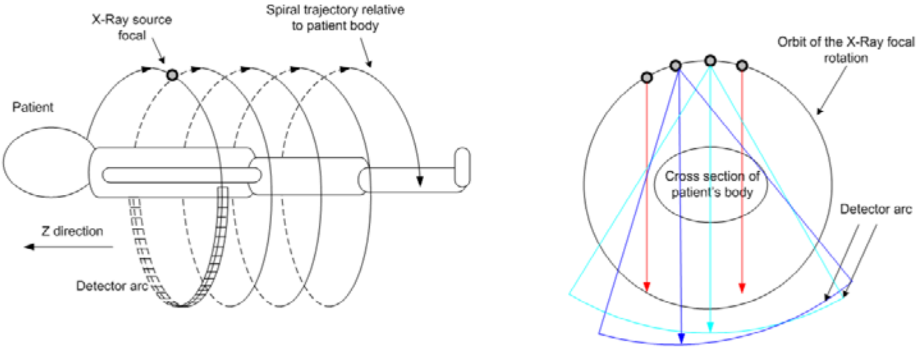


Fig. 4. Concept of spiral scanning; Left: Spiral trajectory of the X-ray source focal point; Right: Interpolated parallel projections.

Though it looks much more complicated than the parallel scanning model, the basic principle is still the same, which is, to acquire the parallel projections (Fig.4, Right) at different angles and solve the attenuation equation. However, since the scanning is spiral, at a give z-axis point, only one projection is available. So an interpolation method, most commonly an average of neighbouring projections, is used to insert the interpolated data.

Solving the inverse Radon transform is similar to the parallel model if the number of the detector rows is less than 4(Cho *et al.* 1993). When there are more than 4 rows of detectors, the measured slices cannot be approximated as perpendicular to the z-axis. Such a case is sometimes referred to as “cone-beam CT” because the X-ray beam can no longer be considered as a fan beam any more. Consequently more complicated data reconstruction algorithms must be employed (Turbell *et al.* 2000, Wang *et al.* 2000, Schaller *et al.* 2000).

The exterior picture of a CT machine is shown in Fig.5. The block diagram of the typical setup of a modern CT system is shown in Fig. 6.

X-ray detectors are mounted on the detector arc, with the arc center overlapping with the X-ray source focal point. Both the source and the detector arc are mounted on a rotating gantry. A slice X-ray filter is applied to absorb the X-ray beam outside the area of interest. In CT terminology, the direction in which the patient table moves is called z-axis direction.

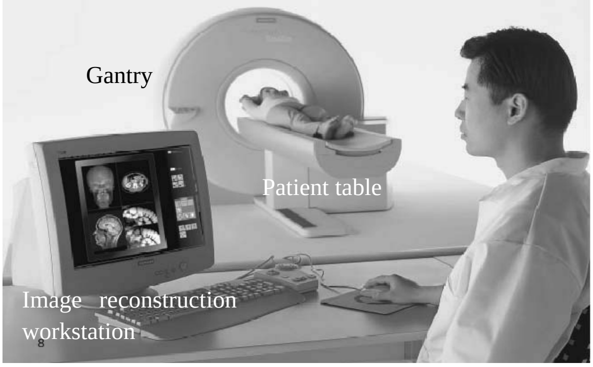


Fig. 5. A CT machine.

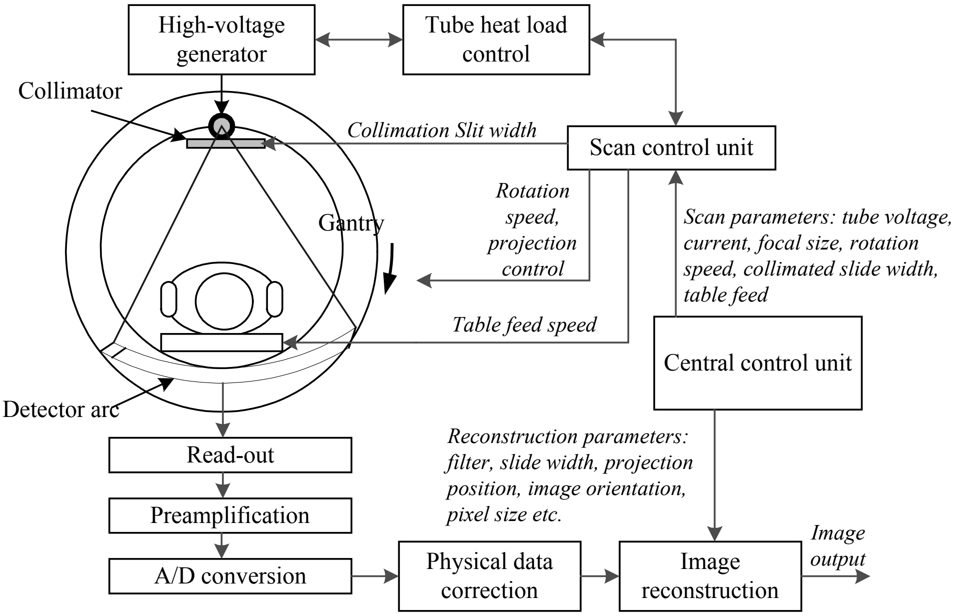


Fig. 6. The block diagram of a typical CT system setup.

The read-out part and the pre-amplifiers convert the current signals from the diode array into voltage signals. In most cases, the pre-amplifiers are an array of transimpedance amplifiers or high-resolution, ultra-low noise current-integration ASICs. After pre-amplification, the amplified voltage signal is converted to a digital signal in the following A/D conversion stage. The basic offset and gain errors which are caused by the detectors and the electronics are corrected at the Physical Data Correction stage. Then the corrected projection data sets are stored in a computer. When all the projections are finished, the restored data are manipulated to reconstruct the image with the principles and algorithms discussed in previous sections.

The patient table feeding speed, the gantry rotation speed, the projection angle and the triggering detector readout are coordinated by the central control unit.

The Tube Heat Control unit monitors the heat dissipated from the X-ray tube to avoid over-heating.

The research work within the scope of this thesis is concentrated on the X-ray detectors.

2.2 General review of modern X-ray CT detector modules

In the early days of X-ray CT, the detector modules were mainly based on direct detection gas detectors. However, following the introduction of high scintillation efficiency, low decay time scintillation materials and silicon photodiode arrays, gas detectors gave ways to solid-state detectors. Almost all modern commercial X-ray CT systems are based on a solid scintillation layer combined with a silicon photodiode array.

2.2.1 Principle of modern X-ray CT detector modules

In this thesis, an X-ray CT detector module is defined as a unit X-ray detector array. Such detector arrays are mechanically mounted side by side and perpendicular to the z-axis to form the detector arc, as shown in Fig. 6 in the previous section. Each module contains a few tens to a few hundreds of active pixels. Each individual pixel converts the incident X-ray into an output current signal.

The cross-sectional view of a modern multi-slice detector module is shown in Fig.7. “slice” is a widely used term in the CT field. It refers to the number of active detector elements in the z-direction. As will be explained in detail later, more “slices” always mean higher scanning speed and better performance.

As shown in Fig.7, a CT detector module mainly consists of 3 parts.

On the top, there is a layer of scintillation material, which turns incident X-rays into visible light. In the CT field, the scintillation screen is commonly referred as the “scintillator”. A scintillator contains an array of elements. Each element corresponds to one active photodiode element, which has nearly the same size. Scintillator elements are optically isolated from each other by a thin layer of opaque material called a reflector. Thus, the light signal generated by one scintillator element contains the information relevant to its specific position.

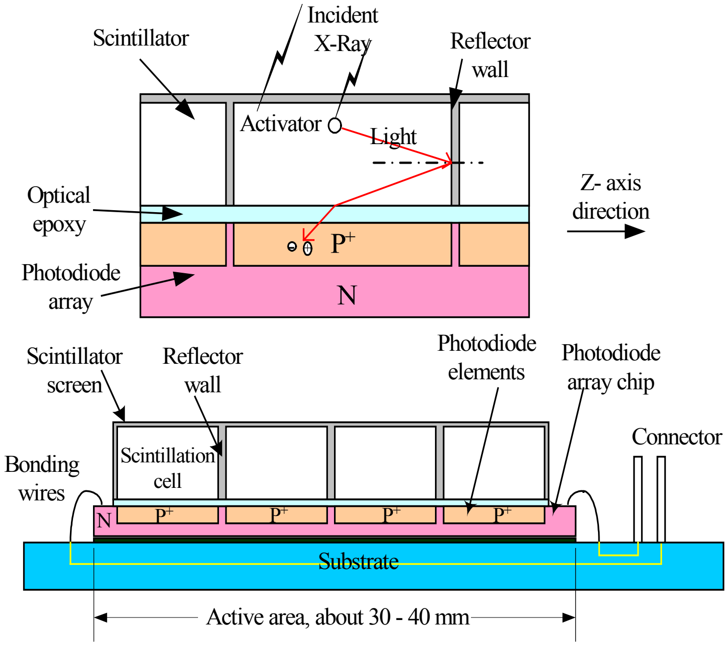


Fig. 7. Cross-section view of a modern multi-slice CT detector module.

The generated light is optically coupled to the corresponding photodiode element in the array by transparent optical compound. The optical compound also serves to mechanically bond the scintillator to the photodiode array. In most modern CT systems, the photodiode elements of one detector array are manufactured on one silicon chip. However, each element has its own active area, electrically isolated from other elements, as will be described later. The photodiode element converts the light signal into a current with an intensity proportional to the light intensity, and thus also proportional to the intensity of the original incident X-ray.

The current output from each photodiode element is led to a bonding pad on the edge of the chip. This in turn it is connected to a pad on the substrate or readout ASICs by wire-bonding.

The substrate is normally made of either high-end PCB (Printed Circuit Board), LTCC (Low Temperature Co-fired Ceramic) or HTCC (High Temperature Co-fired Ceramics). In most cases, the substrate merely serves to connect the signals from the photodiode array to a connector mounted on the substrate, from which the signals are connected to the following stages of the system.

More details of each part of an X-ray CT detector module are discussed in the following sections.

2.2.2 Scintillator

The function of a scintillator is to convert X-rays into light which can be detected by a silicon photodiode. In CT detector modules, only inorganic scintillation materials are employed because they are more stable, and have higher light emission efficiency than organic materials.

A picture of a multi-slice scintillator is shown in Fig.8.

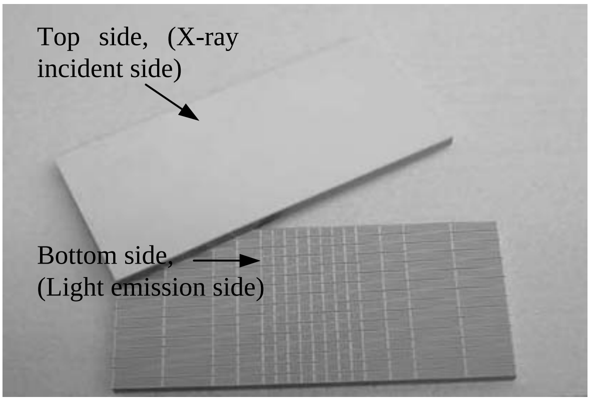


Fig. 8. A multi-slice scintillator, the size is about 40mm x 20mm.

2.2.2.1 Scintillation mechanism

Scintillation materials have an energy band diagram similar to that of semiconductor materials. Electrons constrained inn the valence band can be excited to the conduction band by incident X-rays, creating holes in the valence band. When the excited electrons jump back to the valence band and recombine with holes, their energy is dissipated by the emission of photons with an energy equivalent to the band gap width.

However, in pure crystals the efficiency of the de-excitation process is low and the band gaps are too large to emit light detectable by common light sensors, i.e. photodiodes or PMT tubes. Other materials may be doped to create energy levels inside the energy gap. These doped materials are called *activators*. The energy band diagram of a typical scintillation material is shown in Fig.9. The processes of excitation and luminescence are also shown (Knoll 2000).

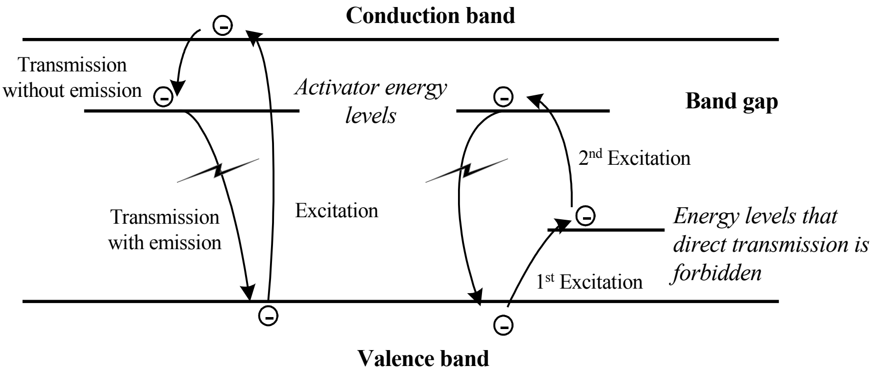


Fig. 9. The energy band structure of an activated crystalline scintillator; On the left hand side there is a normal excitation and emission process. An electron in the valence band is excited to the conduction band. It is then transmitted to the activator energy level without the emission. When it is transmitted from the activator energy band back to valence band, a photon is emitted. On the right the decay mechanism is shown. An electron is excited to an energy level from which the direct transmission to the valence band is forbidden. It has to be activated again to the activator energy band. Then it jumps back to valence band with the emission. This process usually causes a delay of the response from the external excitation, which is called decay.

2.2.2.2 Key characteristics

Emission efficiency, emission peak wavelength, decay time and afterglow are the most importance parameters in characterizing a scintillation material.

The emission efficiency is defined as the ratio of the output light energy to the absorbed radiation energy. It is one of the most important characteristics of a scintillation material. For a wide category of materials it requires, on the average, about three times the bandgap energy to create an electron-hole pair (Knoll 2000). Alkali Halide scintillators, i.e. NaI(Tl), CsI(Tl) and CsI(Na), usually have a higher scintillation efficiency than other materials. When evaluating a material's scintillation efficiency, it is a common practice to quote its light output relative to that of *NaI(Tl)* or *CsI(Na)*.

In most cases, the emission peak wavelength is determined by the *activators*. It is crucial that the scintillation materials have suitable emission wavelengths which overlap or are close to the peak absorption wavelength of the photodiode.

Decay and afterglow cause the same phenomenon, image lag. However, they are due to different causes. Decay reflects the time that it takes for the excited energy states to be de-excited. It is determined by the scintillation material and the activator material and it is a feature rather than a problem. Afterglow is due to another mechanism. When electrons are excited by radiation, some excited electrons are activated to an energy level from which the direct transition to the valence band is forbidden. These electrons have to be further excited to a higher energy state before then can return to the valence band. The further excitation can be provided by, for instance, lattice vibration. Such a mechanism can cause severe lag in the light emission. Afterglow can be caused by the material, by imperfect processing, unintentional doping etc.

Both decay and afterglow are harmful to CT applications because a very high scanning speed is essential in modern CT systems.

2.2.2.3 Main scintillation materials for CT and their key characteristics

Scintillation materials for CT applications are either single crystal cadmium tungstate ($CdWO_4$) or the recently developed ceramic materials based on the rare earth elements, for eample, YGO (Y_2O_3-Gd_2O_3: Eu^{3+}) developed by GE Medical (Duclos *et al.* 2003). GOS (Gd_2O_2S: Pr, Ce, F) developed by Hitachi Metals (Ito *et al.* 1988), and more recently UFC (Ultra Fast Ceramics, composition unavailable) developed by Siemens Medical (Hupke 1998).

In recent years, ceramic scintillation materials have been more and more widely used in CT systems due to their high absorption coefficient, reasonable emission wavelength, ease of machining, low afterglow and short decay (Hupke 1998). $CdWO_4$ was the main scintillation material before the introduction of the ceramic counterparts. Its advantages are good radiation absorption and relatively low decay and afterglow. However, because it is single crystal material, it is not easy to be machined into wanted shapes. It is also brittle and toxic.

A comparison of the key parameters of the four sample scintillators is given in Table 1.

Table 1. Key characteristics of some scintillation material commonly used in CT[*)] *(NA means Not Available).*

	Density (g/cm^3)	Emission λ (nm)	Relative scintillation efficiency	Decay time (μs)	Index of refraction
$CdWO_4$	7.90	530	40	8.9	2.25
YGO	NA	NA	85	1000	NA
GOS	7.34	510	70	4	2.2
UFC	NA	NA	100	3.2	NA

[*)] The data are mainly collected from (Knoll 2000), (Hupke 1998) and (Hupke & Doubrava 1999)

2.2.3 Photodiode and photodiode array

A photodiode is in principle a p-n junction. A photodiode array is an array of p-n junctions made on the same chip. In most cases, it is a 2-D array of isolated p+ implantation or diffusion regions on an n-type substrate. An over-view of a photodiode array and the corresponding electrical symbol are shown in Fig.10.

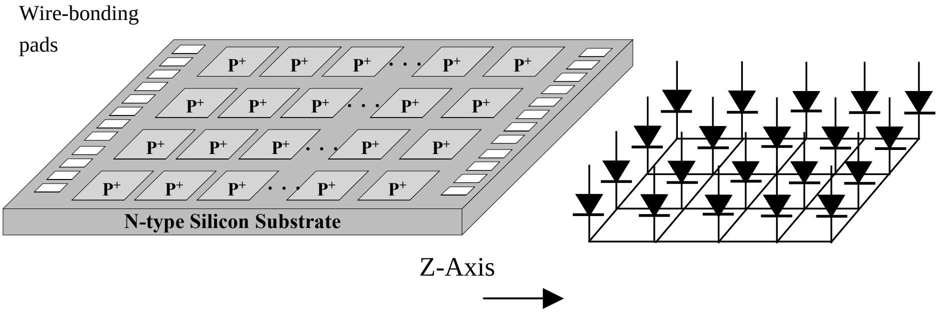


Fig. 10. An over-view of a photodiode array (left); The electrical symbol of the photodiode array (right) .

When a light photon transmits into silicon bulk, it is absorbed by the silicon. The absorption coefficient α describes the fractional decrease in intensity with distance penetrated into a material. It is defined by

$$\alpha = -\frac{1}{I}\frac{dI}{dr} \tag{2.5}$$

where I is the light intensity, which is a function of the penetration depth r.

For a given material, α depends on the incident light wavelength. The shorter the wavelength, the higher the absorption coefficient. The absorption coefficient of silicon as a function of light wavelength is shown in Fig.11.

When a light photon is absorbed by silicon, its energy is transferred to an electron bonded in the lattice, or say, an electron in the valence band. If the energy of the photon is high enough to overcome the energy band-gap, the electron jumps from the valence band to the conduction band. Such a process is called *excitation*. A free electron-hole pair is generated by this process (Sze 2000).

The converse process of photo-excitation is recombination. Thus, if there is no electric field inside the silicon bulk, the generated electron-holes recombine in a very short time after their formation. The p-n junction of a photodiode provides its own internal electric field.

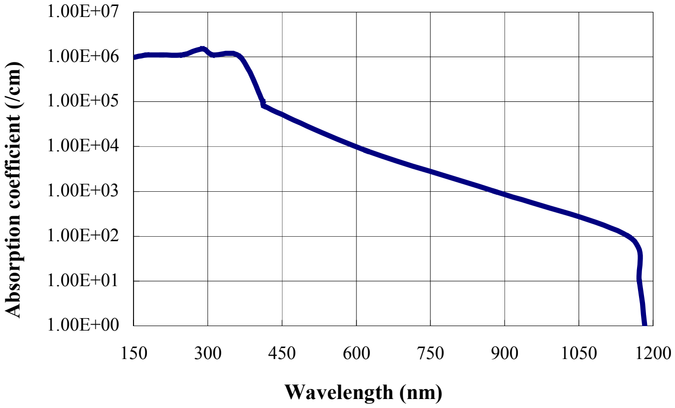


Fig. 11. The absorption coefficient curve of silicon as a function of light wavelength (After Wooten 1972).

A cross-section view of a photodiode element is shown in Fig.12. It shows that light-generated electron-hole pairs can be distributed across the p-n junction. However, only those electron-hole pairs which are generated inside the depletion region, and within one *minority carrier diffusion length* of both the n-side and p-side of the junction can be collected by the p-n junction field and can consequently contribute to the light-generated current.

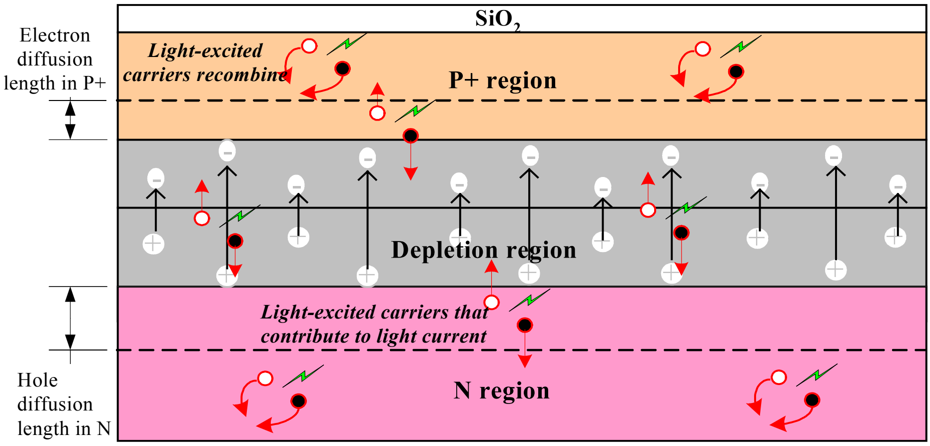


Fig. 12. Cross-section view of a photodiode p-n junction.

Quantum efficiency and light sensitivity are the two parameters that reflect the efficiency of a photodiode in converting a light signal into an electrical signal.

Quantum efficiency is defined as the number of effective electron-hole pairs divided by the number of incident light photons. The term “effective electron-hole pairs” means those electron-hole pairs collected by the electrodes.

$$\eta(\nu) = \frac{I_{photo}/q}{P_{light}/h\nu} \tag{2.6}$$

where I_{photo} is the light generated current intensity; q is the electron charge; P_{light} is the power of the incident light; h is the Planck’s constant; ν is the frequency of the incident light.

Light sensitivity is defined as the light-generated current intensity divided by the incident light power,

$$S = \frac{I_{photo}}{P_{light}} \tag{2.7}$$

So the quantum efficiency and the light sensitivity are directly linked to each other. Their relation can be determined by

$$\eta = \frac{S \cdot h\nu}{q} \tag{2.8}$$

The quantum efficiency and light sensitivity are mainly determined by the absorption coefficient, and the depletion region depth.

Dark current, or leakage current, is defined as the current output from the photodiode when there is no incident light or radiation or any other external excitation.

Dark current is created by a thermal excitation process, which is similar to the photo-excitation process except that the excitation source is thermal energy instead of photon energy. Because the energy acquired from lattice thermal vibration at normal operation temperature is usually much less than the band gap energy, thermal excitation and recombination can only happen at impurity energy levels inside the band gap. The dark current density J_s is exponentially dependent on the temperature (Liu *et al.* 1994).

$$J_s = \frac{qD_n n_{p0}}{L_n} + \frac{qD_p p_{n0}}{L_p} = q\left(\frac{D_n}{\tau_n}\right)^{1/2} \frac{n_i^2}{N_a} + q\left(\frac{D_p}{\tau_p}\right)^{1/2} \frac{n_i^2}{N_d} \propto T^{3+\frac{\gamma}{2}} \exp(-\frac{E_g}{kT}) \tag{2.9}$$

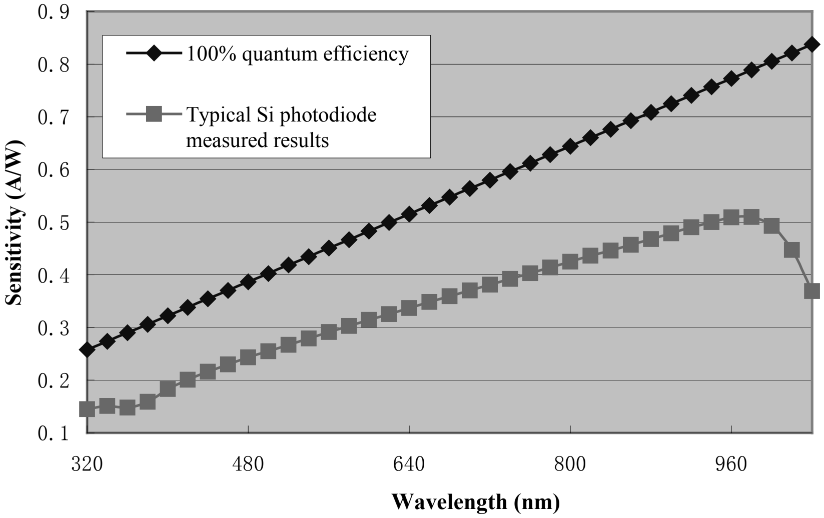


Fig. 13. A typical photodiode light sensitivity compared to the theoretical maximum sensitivity assuming 100% quantum efficiency.

where D_n, τ_n, L_n, D_p, τ_p, L_p are the diffusion coefficient, minority carrier lifetime and diffusion length of electrons and holes, respectively; n_{p0} and p_{n0} are the electron density in the p region and hole density in the n region at equilibrium; n_i is the carrier density in intrinsic silicon; N_a *and* N_d are the doping density in the p region and the n region respectively; E_g is the silicon band gap width; γ is a constant that satisfies

$$\frac{D_{n,p}}{\tau_{n,p}} \propto T^{\gamma} \tag{2.10}$$

Dark current has three negative effects on a CT system.

1. Dark current is an offset in the system, so it occupies a fraction of the dynamic range of the electronics;
2. Dark current introduces in quantum noise due to its fluctuation;
3. Dark current is exponentially dependent on temperature. Thus fluctuation of the dark current caused by temperature variation will mislead the image by being taken as a fluctuation of the wanted signal.

Dr. H. Wang reported in his thesis a dark current density of 80pA/cm^2 at 10mV bias, which was reported the lowest at that time (Wang 2001). As will be discussed later, a lower average dark current density is achieved in this thesis.

However, in CT applications, the negative effects of the dark current are not as significant as in the safety and security applications presented by Hongbo. In CT applications, the radiation dose is much higher than in the safety and security applications. Consequently, the signal level is also much higher. A typical photodiode output current can be in the order of 100nA to a few uA, while the photodiode dark current is typically lower than 1pA to a few pA at 10mV bias, depending on the size of the photodiode. Another reason is that the medical CT system application environment is almost room temperature, e.g. the environment temperature inside the detector chamber is usually less than 40 degrees. Thus the dark current fluctuation due to temperature variation is limited.

Photodiode noise has two sources (Wang 2001).

1. Fluctuation of the thermal dark current is given by

$$I_{noise,leakage}(\Delta f) = \sqrt{2qI_{leakage}\Delta f} \tag{2.11}$$

Substitute $I_{leakage}$ with 1pA, and Δf with 1MHz, which is defined by the bandwidth of the pre-amplification stage. The noise of the dark current is then

$$I_{noise,leakage}(10^6) \approx 0.56pA \tag{2.12}$$

2. Johnson noise of the parasitic series resistance

The typical value of the parasitic series resistance of a CT photodiode element is in the range of a few ohms to a few tens of ohms. Thus, Johnson noise caused by the parasitic resistance is also small.

As will be discussed in a later chapter, photodiode noise is negligible compared with other noise sources. It is not the dominating noise source of a CT.

Photodiode capacitance and resistance play a key role in determining the performance of the CT system.

The capacitance and resistance model of a photodiode element in a photodiode array is shown in Fig.14.

The capacitance of each element in a photodiode array is made up of three parts.

1. p-n junction capacitance

The diode junction capacitance contains the depletion layer capacitance and the diffusion capacitance.

When the external bias is zero, the depletion layer capacitance is given by (Taur & Ning 2000)

$$C_j = A\frac{\varepsilon_{si}}{W_d} = A\sqrt{\frac{q\varepsilon_{si}N_aN_d}{2(N_a+N_d)\psi_m}} \tag{2.13}$$

where A is the area of the depletion region, W_d is the thickness of the depletion region, N_a and N_d are the impurity density in the p-region and n-region respectively; ψ_m is the built-in potential drop at the p-n junction and is defined by

$$\psi_m = \frac{kT}{q}In(\frac{N_aN_d}{n_i^2}) \tag{2.14}$$

For a p^+n junction, at low frequency the diffusion capacitance is given by equation (2.15) (Liu 1994)

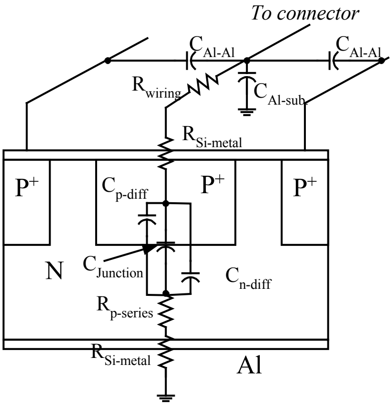


Fig. 14. The capacitance and resistance model of one element in a photodiode array.

$$C_D = \left(\frac{Aq^2 p_{n0} L_p}{k\,T}\right) \exp\left(\frac{qV}{k\,T}\right) \tag{2.15}$$

where A is the area of the junction; L_p is the hole diffusion length inside the n-region; V is the forward bias; p_{n0} is the hole density in the n region at equilibrium, which can be determined by

$$p_{n0} = \frac{n_i^2}{N_d} \tag{2.16}$$

where n_i is the intrinsic carrier density and N_d is the impurity density.
The total output capacitance of a diode is the sum of these two parts. The value varies from a few *pF* up to more than one hundred *pF* depending on the application.

2. Parasitic capacitance of Al lines to the bulk

The parasitic capacitance of the Al lines to the bulk is made up of two parts in series, the oxide layer capacitance and the depletion layer capacitance formed by the depletion region under the Al lines.

The oxide layer capacitance contains a parallel-area component and a fringing-field component. It can be estimated according to Schaper and Amey's model (Schaper *et al.* 1983). If the oxide thickness is 0.5μm, and the line width is 10μm, the oxide layer capacitance is close to 4pF/cm.

The depletion layer capacitance is given by (Taur & Ning 2000)

$$C_{d-para} = A\frac{\varepsilon_{si}}{W_d} = A\sqrt{\frac{q\varepsilon_{si}N_d}{2V_{appl}}} \tag{2.17}$$

where A is the area of the depletion region; W_d is the thickness of the depletion region; N_d is the impurity density in the n-type substrate, V_{appl} is the potential difference between the Al line and the substrate.

Since in most cases the lines are zero biased, any bias on the substrate is from the oxide charges. It is negligible in this case.

In a multi-slice detector module, the middle elements have the longest wiring distance among all the elements. It is about half of the length of the die, which is about 25mm. Thus the worst-case wiring parasitic capacitance is about 10*pF*– 20*pF*.

3. Parasitic capacitance of neighbouring Al lines

The parasitic capacitance of neighbouring Al lines can also be estimated by Schaper and Amey's model. (Schaper *et al.* 1983) By referring to the commercial CMOS processing parameter, the capacitance between 25mm long neighbouring Al lines would be in the order of sub-pico farads, assuming the line width to be equal to the line spacing.

The resistance of each element in a photodiode array contains the inherent resistance and the parasitic resistance.

The inherent resistance includes the metal-silicon contact resistance on both the top and bottom sides and the bulk series resistance of both the n- and p- doped region. The typical inherent resistance of one element is from several ohms to over ten ohms.

The parasitic resistance is mainly the Al wiring resistance. It is given by

$$R_{wiring} = \frac{L_{wire}}{W_{wire}} \cdot R \tag{2.18}$$

where L_{wire} is the total length of the line; W_{wire} is the width of the line; $R_{\square}$ is the square resistance of the Al lines. In a typical detector process, $R_{\square}$ is around 50mΩ/□. The line length for the middle elements is about 25mm. The typical line width is 8μm. The wiring resistance of the middle elements is about 156Ω, which is more than ten times the inherent resistance.

The photodiode capacitance and resistance have several negative effects on the system level performance of a CT system.

High photodiode capacitance raises the noise level in the CT pre-amplification stage because the pre-amplifier noise is proportional to its input capacitance. The details are discussed in later chapters.

The parasitic capacitance between neighbouring elements couples the signal from one element to its neighbour. This is an important source of signal cross-talking, which has negative effects on imaging.

The parasitic resistance and capacitance cause an RC delay in the pre-amplification stage, which is a potential limit to the system response speed. However, since the integration time in present CT systems is usually a few hundred *μs*, the RC delay is negligible unless the parasitic R and C components are very large.

In summary, the key characteristics of photodiodes for CT application are as follows.

i Light sensitivity. This determines the current intensity for a given light intensity. The sensitivity depends on the silicon processing technology.

ii Photodiode capacitance, including the photodiode junction capacitance and the wiring parasitic capacitance. The higher the capacitance there is, the higher the noise level that can be expected in the pre-amplification stage.
iii Dark current and series resistance.

2.2.4 Substrate

The substrate and the corresponding die-bonding technique play key roles in manufacturing costs, yield and long-term reliability.

The requirements for a good CT detector module substrate include good surface flatness, low tilt, precise mechanical dimensions, low CTE (coefficient of thermal expansion), the capability of integrating multi-layer high-density wiring and small-sized vias, and low costs for mass production.

Poor surface flatness and tilt cause stress in the silicon chips during the assembly process and throughout their lifetime, as shown in Fig.15. After die-bonding with such a substrate, the curved top surface of the silicon die will make the scintillator assembly process very difficult.

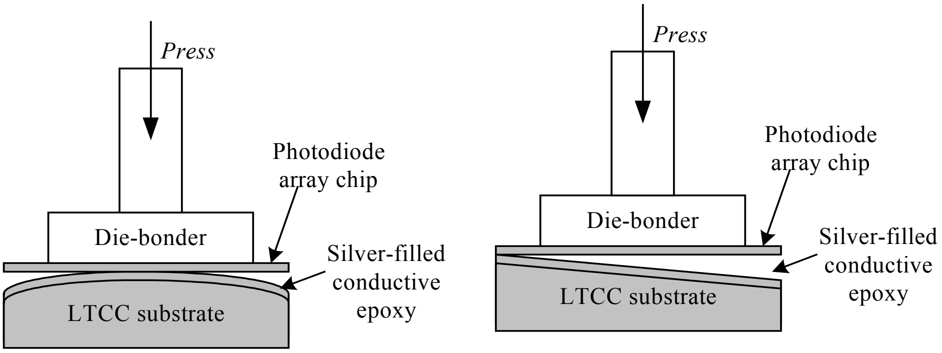


Fig. 15. Substrate with bad surface flatness and tilt.

High mechanical precision in the substrate dimensions, mount hole sizes and positions is are also crucial. When the detector modules are mounted side by side to form the detector arc, the same pitch size has to be maintained on the edges with an accuracy of about two hundred microns.

Any CTE mismatch between the silicon die and the substrate should be kept as small as possible to minimize the stress. Due to the large size of the silicon die, the displacement can be significant even for a relatively small CTE mismatch.

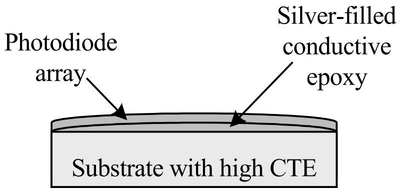


Fig. 16. Silicon photodiode array assembled on a substrate with high CTE can cause high stress in the silicon die.

The CTE data of some materials discussed in this thesis are shown in Table.2.

Table 2. CTE of some typical material.

	Si	FR4	LTCC
CTE (ppm/℃)	2.8	18(x,y); 50 (z)	7.0 (Dupont material)

In the module assembly process, the temperature variation is normally around 100℃. The size of a silicon die in the z-direction is around 50mm in modern systems. If FR4 material is used, the displacement caused by the CTE mismatch would be about 38μm from each side.

$$D_{Dislocation} = \Delta T \cdot (CTE_{FR4} - CTE_{Si}) \cdot L = 100 \times (18 - 2.8) \times 10^{-6} \times 50 = 76\mu m \qquad (2.19)$$

As explained previously, a curved surface makes it difficult to attach the scintillator. The mechanical stress due to the displacement is also high, which consequently leads to poor long-term reliability.

Due to the large amount of elements, a huge number of routeings are required on the substrate. As an example, a 32-slice module would have at least 512 individual routes (32 x 12) on the substrate and these routes have to be within the very limited physical area. Thus, high-density, high-resolution wiring and small-sized vias are required.

Substrates made of HTCC (high temperature co-fired ceramics) or LTCC (low temperature co-fired ceramics) and special PCB (printed circuit board) materials are commonly used in modern multi-slice CT detector modules.

LTCC is a relatively new processing technology used in microelectronics packaging, especially RF component packaging. Its manufacture is performed in two steps. Firstly, manufacture of the so-called green tapes. A slurry is prepared by mixing ceramic powder and the vehicle containing surfactant, binders and plasticizers. The slurry is tape-cast into a thin layer with uniform thickness. After the binder materials have been driven off by heating, the film is solidified into green tapes. Secondly, the green tapes are formed into the required shapes. Via holes are then drilled and conductive paste is filled into the holes. Conductive paste is also printed onto the tape to make the routeing traces, as in

PCB manufacturing. When all the layers are printed, they are aligned, laminated and fired to yield a rigid substrate (Hu 2004, Jantunen 2001, Jakku 2003).

Conventional FR4 PCB material is not suitable for CT detector module substrates. This is not only because of its high CTE, but also its high dielectric coefficient and its inhomogeneity in both mechanical and electrical properties. However, special PCB materials which are not based on a fiber framework can be used as CT detector substrates. There are many of them commercially available (Tummala 2001).

LTCC is chosen in this study because of its excellent dielectric property, excellent mechanical properties, and also because of the extensive experience we already have of this material and the associated processes. It is believed, but not tested, that the novel detector micro-module in this study could also be manufactured on the special PCB substrates mentioned above.

2.3 Evolution of spiral CT detector modules

The X-ray detector modules for spiral CT systems have evolved over three generations since the introduction of spiral CT systems.

- 1st generation spiral CT detector module, single-slice detector module

  In the early spiral CT system, or say, the first generation of spiral systems, the detector modules were so called “single-slice modules”, which means that there is only one row of detector elements in z-axis direction. A diagram of the single-slice module and the detector arc composed of single-slice modules are shown in Fig. 17.

  As shown in Fig.17, the physical dimension of a detector element in the z-axis direction is much longer than in the perpendicular direction. The actual scanning pitch can be chosen by adjusting the collimator opening width. In clinical practice, the doctor may intend first to rapid-scan a large volume of a patient’s body in order to locate the area of interest. In this case, the scanning time rather than the image resolution is the key factor. Consequently, a rough scanning pitch in z-axis direction is engaged. After the pathological focus is located, a slow and fine scan is carried out only over the pathological focus area. For the fine scan, a finer element pitch is preferred to achieve higher image resolution.

  A single-slice detector module is simple and easy to manufacture but the fine scan takes long time. For example, the typical length of a lung is around 300mm. If the lung is scanned with fine collimation (typically 1 mm collimation; 1 second/rotation; pitch factor 1.5, i.e., a 1.5mm table feed per rotation cycle), the scanning time is 200s as given by equation 2.20.

  $$T_{scan} = L_{scan} / (\text{collimation pitch x pitch factor}) = 200\text{s} \tag{2.20}$$

  It is not possible for a patient to hold breath for 200 seconds. In other words, a larger collimation pitch has to be used, which in turn means a lower image resolution.

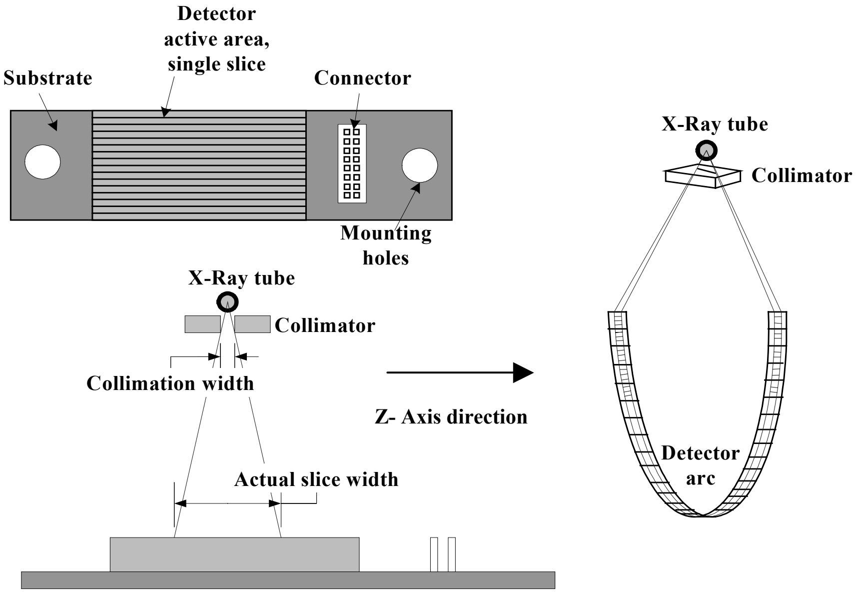


Fig. 17. The diagram of the single-slice X-ray CT detector module; Up: Top view; Right: An X-ray CT detector arc composed of single-slice modules; Low: The actual slice pitch is determined by collimator opening width.

- 2nd generation spiral CT detector module, dual-slice detector module
  In order to improve the scanning speed, dual-slice detector modules were introduced. In dual-slice modules, there are two rows of detector elements in the z-axis direction. Thus two rows of data can be acquired at the same time. Compared with single-slice modules, the period required for a fine scan can be improved by 100% with the same image resolution.
  A sketch of a dual-slice module, a dual-slice module detector arc and the way to adjust the actual collimation pitch are shown in Fig. 18.

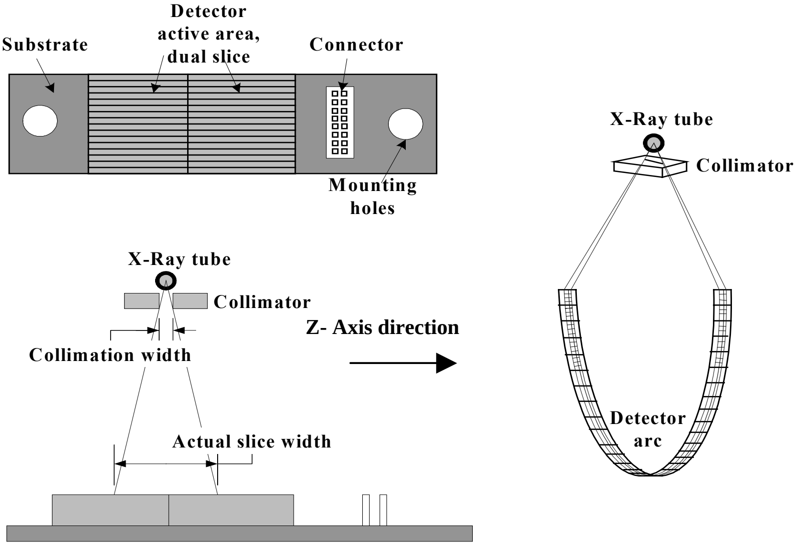


Fig. 18. The diagram of a dual-slice X-ray CT detector module; Up: Top view; Right: An X-ray CT detector arc composed of dual-slice modules; Low: The actual scanning pitch can be determined by collimator opening width.

3rd and current generation spiral CT detector module, multi-slice detector module
The multi-slice module and the detector arc composed of multi-slice modules are shown in Fig. 19.

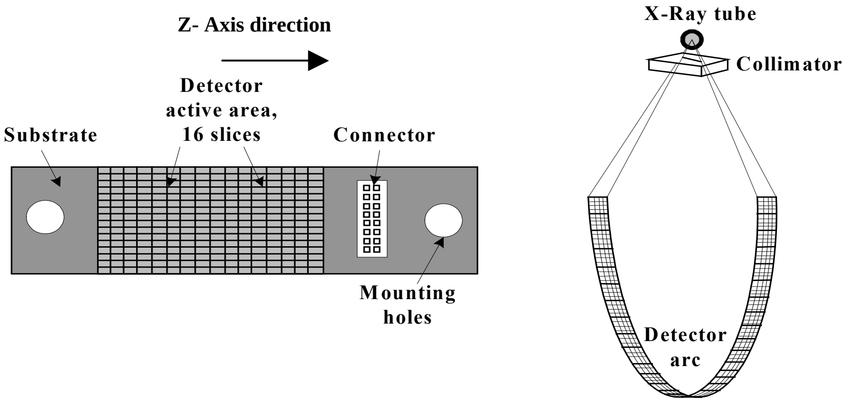


Fig. 19. The diagram of a multi-slice X-ray CT detector module; Left: Top view; Right: An X-ray CT detector arc composed of dual-slice modules.

The relation between the scanning period and the number of slices is shown in equation 2.21.

$$t = \frac{d}{p \cdot M \cdot S} \cdot t_{cycle} \qquad (2.21)$$

where t is the total period of one scan; d is the total scanning length; M is the number of slices; S is the pixel pitch; p is the pitch factor, normally 1.5; t_{cycle} is the time period for the gantry to rotate for one cycle.

In the case where the gantry rotation speed remains constant (i.e., pitch factor and pixel pitch are kept the same), and the image resolution remains constant, the time period required to scan the same distance is decreased by a factor of M.

If we take the same lung scan described in the case of the single-slice module as an example, scanning the whole lung with the same 1-mm-collimation using 16-slice detector modules would take only about 12 seconds.

Shortening the scan time span not only means higher throughput and consequently higher cost-efficiency, although this is also an important point. The more important fact is that a short scanning time opens up more application fields for CT systems.

As shown by the lung scan example, with single-slice modules, the time interval for one scan is 200 s, which makes it impossible for most patients. With 16-slice modules, the time is 12 seconds which is suitable for most patients. However, this is still not suitable for those who can not hold their breath at all, for instance, those patients who are unconscious. However, with 32-slice, or 64-slice modules, it will be possible.

A more difficult application is angiographic and cardiopathic diagnosis. Here, even faster scanning is required because a normal beat takes only 0.5 – 1s, which requires a scan time of less than 0.05s (Bonnet *et al.* 2003).

A greater number of slices also introduces the possibility of using smaller detector element pitch and hence improve the image resolution. This can also be explained in equation (2.21). The total allowed scan time t is determined by the application. (e.g. by the time that the patient can keep still, and by the cost). d is determined by the area to be scanned. Assuming that the cycle time for one rotation $t_{cycle,}$ is constant, then obviously, with higher M, there is more scope to reduce p and S, which are the two key factors in determining the image resolution.

Nowadays, the most popular CT systems normally have 16 slices, and these will be used as the benchmark reference in this thesis. There are already 24-slice commercial products in existance. 32-slice systems are under development.

2.4 Typical assembly process

The main assembly steps are shown in Fig.20.

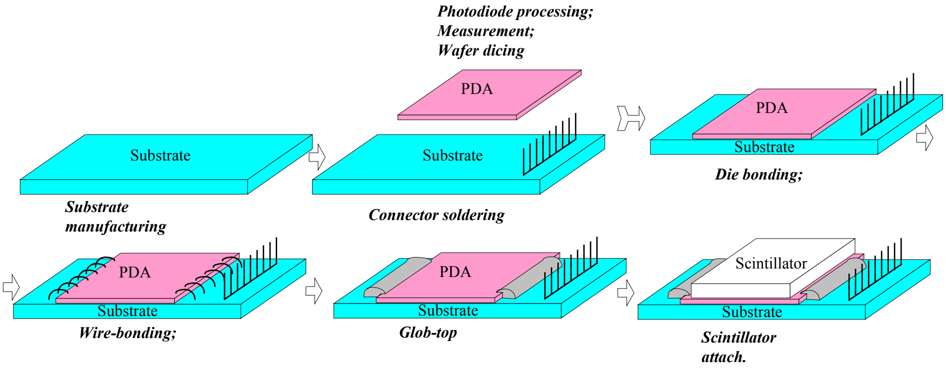


Fig. 20. The main assembly steps for a multi-slice CT detector module.

1. Connector soldering

Connector soldering is normally the first assembly step because the following assembly steps cannot withstand the reflow temperature which is around 220℃

2. Die bonding

Die bonding is used to place the silicon dies, i.e. the photodiode array and Ics, if any, onto the substrate. Conductive epoxy (silver-filled) is normally used to give conductive as well as mechanical bonding between the dies and the substrate. The assembly precision, treatment of the conductive epoxy, bonding force, bonding time and curing conditions are the key issues in the die bonding process.

3. Wire-bonding

Due to the large number of detector elements, and the limited available space, the wire-bonding density can be very high, as will be revealed in a later chapter.

4. Glob-top

“Glob-top” is to protect the bonding wires and ICs from external physical damages. It is applied by dispensing non-conductive glob-top epoxy onto the area to be protected.

5. Scintillator attachment

Scintillator attachment is the key step required to achieve optimal optical coupling and mechanical bonding between the scintillator and the photodiode array. This is normally done by placing the scintillator onto the silicon die with a gap around 100 μ m between them. Transparent epoxy material with very low viscosity is then fed into the gap. With the help of the capillary force, the epoxy spreads all through the gap and over the surface of the silicon die. The epoxy is then cured.

2.5 Limits with the present approach

Throughout the evolution of the CT detector, the basic methodology of building a detector module and the detector arc has changed very little. In short, the methodology is to place identical detector modules side by side along the direction perpendicular to the z-direction. Within a detector module, each individual detector element has a conductive line connecting the element to a bonding pad which is on either of the two edges of the photodiode array chip. The bonding pads are then wire-bonded to corresponding pads either directly on the substrate, or in some cases, a read-out ASIC. The wire-bonding pads on the substrate, or the outputs of the ASIC chips are then connected to connectors on the same substrate. Such a methodology was shown in Fig.10, Fig.17, Fig18 and Fig.19 in previous sections.

However, with such methodology, it is very hard, if possible at all, to build detector array with 64 or more slices because of its inherent problems.

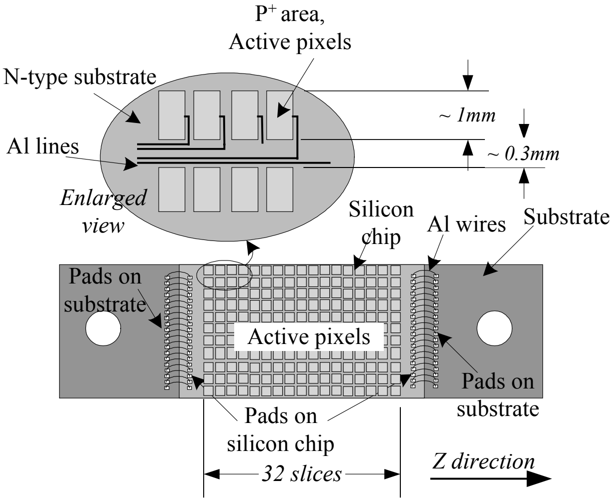


Fig. 21. Top view of an isotropic 32-slice detector module.

The problems are revealed in Fig.21 with an isotropic 32-slice detector as an example. The term *isotropic* module means all pixels have the same pitch size in the z-direction. Otherwise they are called *adaptive* detector modules. The following discussion also applies to *adaptive* modules.

The inherent problems with the current approach are summarized as follows.

- Wire bonding density
  With an increasing number of slices, wire-bonding becomes more challenging due to the high bonding wire density. The upper limit will be reached when the number of slices reaches 64, which is expected by the CT industry to be within a few years' time.

64-slice modules have 64 detector elements in the z-axis direction. On either end of the silicon die, within the space of one element pitch, which is typically around 1mm, there are at least 32 bonding wires.
Bonding wire spacing is then given by

$$\frac{p_{element}}{N_{wires}} = \frac{1mm}{32} \approx 0.031mm \tag{2.22}$$

where $p_{element}$ is the detector pixel central pitch value in the z-axis direction; N_{wires} is the number of bonding wires within one element pitch.
This is already close to the diameter of ordinary Al-Si bonding wire, which is 25µm. To keep enough space between neighbouring wires, the wires have to be bonded in 3 or 4 layers. Because the bonding pads' pitch has to be maintained around 100µm, bonding pads have to be placed into 3 - 4 columns. Eventually the bonding will become very complicated. This complexity increases the manufacturing cost and decreases the manufacturing yield. It is not practically possible to produce detector modules with more than 64 slices with this methodology.

- Parasitic wiring capacitance
  The detector elements in the central part of the module have significantly longer lines than those on the edges. High parasitic resistance and capacitance thus occur with the central elements. As discussed in a later chapter, the noise level in the pre-amplification stage is proportional to the diode capacitance. Consequently, the parasitic capacitance degrades the noise performance of the central elements. More detailed discussions on the parasitic capacitance are given in later sections.

- Reduction on active area
  Wiring occupies valuable active area and this eventually degrades the imaging resolution. This is shown in the zoom-in picture in Fig.21.
  The typical value of detector element pitch is around 1mm. If the conductor line pitch is 20µm, it can easily be calculated that a 32-slice detector module loses about 32% of its active area because of the wiring. Similarly, a 64-slice module loses about 64% of its active area if the element pitch and the trace pitch remain the same.
  The trace pitch can be decreased to preserve the active area ratio. However, this is at the cost of lower production yield, higher manufacturing costs and higher parasitic effects.

- Cross-talk
  When the routeing density is very high on the chip, parasitic capacitance between neighbouring channels is high and may cause serious cross-talk problems, which in turn may spoil the image quality.

Following a careful study, the conclusion is made that 64-slices will be the ultimate extreme of the current approach to manufacturing the CT detector module. A breakthrough is needed to meet the requirement of multi-slice detector modules from the CT industry.

2.6 Review of contemporary potential solutions

Various methods, concepts and technologies have been proposed to achieve this breakthrough. However, till now, there is no commercial product, nor any method which can solve all the problems and at the same time incur a reasonable manufacturing cost. From an up-to-date literature survey, the most investigated solution is to apply a flat-panel detector array to CT imaging. Other publicly known solutions include the active-pixel solution proposed by Yasuo Saito in Toshiba Medical (Saito *et al.* 2002) and the back-illuminated diode array by R. A. Mattson in Philips Electronics (Mattson & Vrettos 2002).

2.6.1 Flat-panel detector

There are two kinds of flat-panel detector arrays; direct- and indirect- detection. Direct-detection flat-panel detectors are made of an amorphous selenium layer in which electron-hole pairs can be directly activated by X-ray photons. However, a very high voltage, 1000-5000 volts, is required to operate this direct-detection flat-panel detector, and its *Detective Quantum Efficiency* (DQE) is also reported to be low (Partridge *et al.* 2002). More widely investigated is the indirect-detection flat-panel detector, shown in Fig.22.

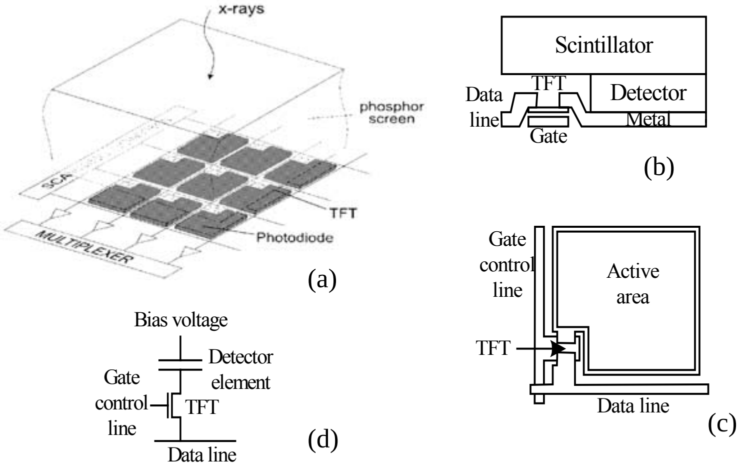


Fig. 22. Structure of an indirect-detection flat-panel detector; (a) Overview of the detector array (Rowlands 1998); (b) Cross-section view of one detector pixel; (c) Top-view of one detector pixel; (d) Electrical symbol of one detector pixel (Rahn *et al.* 1999).

The working principle is briefly as follows. Incident X-rays are absorbed by the phosphor screen and transferred into visible light which is absorbed by the amorphous photodiode array. Electrical currents are created in each element and charge the capacitor of the sensor to a value near to the bias voltage.

Each column of the array shares the same data line and each row of the array shares the gate line, or say, the control signal. When one row is chosen by the control circuit, the signals on each column are amplified at the same time and read out in series.

The timing control circuits and the readout circuits are ASICs which are bonded at the sides of the array.

Because flat-panel detectors are manufactured by thin film deposition on glass substrates, the size of the detector array is not limited by the silicon wafer size, as are single-crystal detectors do. The reported detectors have sizes from about 21.5 x 21.5 cm^2 to 43 x 43 cm^2 (Knupfer *et al.* 1999). With a TFT read out circuit, it is relatively easy to access to a large quantity of elements by reading them line by line. The wire-bonding problem discussed in Section 2.5 is diminished.

Other benefits with flat-panel detectors are fine pitch size (Rahn *et al.* 1999); high active area ratio (Rahn *et al.* 1999); reasonable linearity (Antonuk *et al.* 1998); and a high spatial resolution (Darambara *et al.* 2002).

The flat-panel was first introduced as an X-ray diagnostic device. Attempts have been made to apply the detector to CT imaging systems (Jaffery *et al.* 2002, Ruchala 1999, Antonuk *et al.* 1998, Ning *et al.* 2000).

However, there is still a long way to go before flat-panel detectors can replace single crystal photodiode arrays in conventional CT systems. Flat-panel detectors suffer serious drawbacks because of the imperfection of α:Si-H crystal structure.

- Long image lag
  Due to the imperfection of the α:Si-H crystal structure, a significant number of light-generated carriers are trapped inside the film. Some of these carriers are released afterwards, causing long image lag. The best reported image lag performance is 1% at 100ms after exposure (Partridge *et al.* 2002). This is extremely long compared to the integration time of a few hundred µs to a few ms in conventional CT applications.

- High noise and low dynamic range
  Again mainly due to the imperfection of the α:Si-H crystal structure, high noise and hence low dynamic range is reported in every flat-panel device.
  The best reported dynamic range is about 13 bits (Hosch *et al.* 2002). This is encouraging, but still far from the 18-20 bits of dynamic range required by CT systems.

- Image distortion due to cone-beam illumination on a flat plane
  Due to its large and flat shape, the X-ray dose at the centre and the edge of the detector are different. The corresponding image pitch sizes are also different, as shown in Fig.23. Without correction this will causes severe image distortion. Correction algorithms have been developed to alleviate this problem but this is at the expense of more computation load.

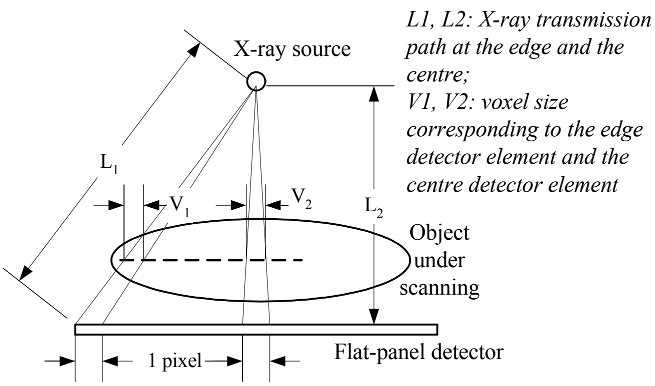


Fig. 23. Image distortion due to cone beam illumination.

In summary, although the flat-panel solves the detector size problem and achieves a very fine pitch size, due to the imperfection of the crystal structure, its severe image lag and limited dynamic range prevent it from replacing the single crystal detector array in the foreseeable future.

2.6.2 Active-pixel detector

M. Endo *et al.* introduced the concept of the active-pixel detector in 2001, which they referred to as “4-D CT” (Endo *et al.* 2001). The concept was patented in 2002 (Saito *et al.* 2002).

After two years’ development, recently a prototype CT system with the proposed active-pixel detector has recently been developed. A preliminary performance evaluation has been made (Endo *et al.* 2003, Endo *et al.* 2002, Endo *et al.* 2003).

The active-pixel detector has a similar read-out concept to that of the flat-panel detector does. The basic building block of the active-pixel detector is shown in Fig.24.

As shown in Fig.24, inside each pixel there is an embedded MOS switch. The gate of all MOS switches in each row is controlled by a common line from a shift register. Each column shares a common data line. As in the flat-panel detector, data are read out row by row.

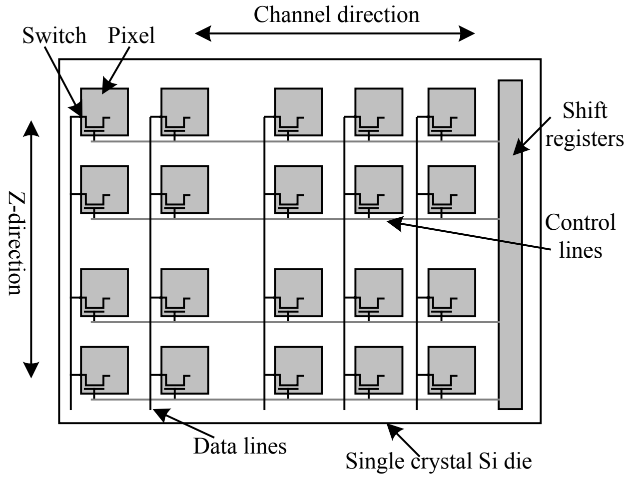


Fig. 24. Diagram of the active-pixel photodiode array (after Endo *et al.* 2003).

A full detector array is composed of many such building blocks. It is shown in Fig.25. Space is left for one row of wire-bonding pads on the edge of each block. The scintillator edge is wedged to leave space for wire-bonding. The data lines and the control lines are connected to the substrate via wire-bonding.

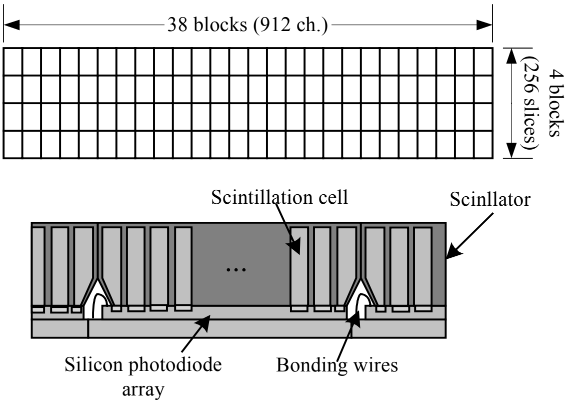


Fig. 25. The upper one: Active-pixel detector array built by building blocks, the reported CT system has 38 x 4 building blocks with each block containing 24 x 64 detector pixels (After Endo *et al.* 2004, Fig.2); The lower one: Enlarged cross-section view of the edges of the building blocks; (After Saito *et al.* 2002, Fig.6).

In summary, by using the row-by-row readout concept, the number of wire-bonding pads, and hence the required wire-bonding space is reduced. By wedging of the scintillator, active area covers the full module, and hence building blocks can be tiled together to form bigger detector arrays.

The active-pixel detector is a promising method to realize next-generation CT. However, there are also a few challenges to overcome.

The electrical symbol of one individual pixel is shown in Fig.26.

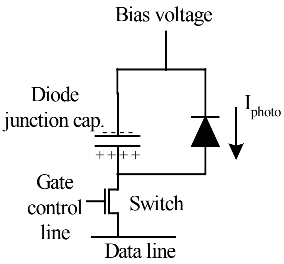


Fig. 26. Electrical symbol diagram of an active-pixel detector pixel.

During most of the time in a readout cycle, the switch is open. Thus the light-generated current will create a voltage across the diode junction, which is equivalent to a forward bias to the diode. This forward bias decreases the junction depletion region width and degrades the light sensitivity of the diode pixel. As a result, the light sensitivity of every pixel is not linear and is signal-dependent. The higher the signal level, the lower is the sensitivity. This may have negative effects on the imaging quality when signal level is relatively high.

Manufacture of the wedged scintillator shown in Fig.25 might be costly. Integrating MOS processing technology into detector processing technology makes the processing steps somewhat more complicated.

2.6.3 Back-illuminated photodiode array

The concept of a back-illuminated photodiode array was introduced and patented by R. A. Mattson in 2002. (Mattson & Vrettos 2002)

The principle is shown in Fig.27. The feature of the invention is to use the “back side” of a photodiode array as the light sensitive surface. Thus the “top side” can be used freely for routeing and bonding. In this way, the limitations discussed in Section 2.5 are avoided. Many modules as shown in Fig.27 can be tiled to form bigger detector arrays.

However, there are also a few bottlenecks with this concept.

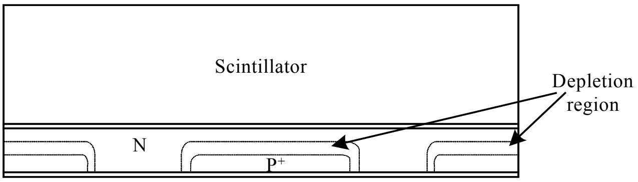


Fig. 27. Cross-section view of a back-illuminated X-ray detector with photodiode array.

The main bottleneck is that the light absorption region is far away from the carrier collection region. As discussed previously, light is absorbed a few micros into the silicon bulk. Thus most light-generated carriers are generated within a few microns of the incident border. For the “back-illuminated” photodiode, this is the region close to the “back surface”. However, the carriers must be collected by the junction electrical field, which is on the “top” side of the diode. Since the normal wafer thickness is a few hundred microns, the carriers have to travel this distance to reach the electrical field. In view of the diffusion length being a micron, the quantum efficiency will be low becuase a large percentage of the light-generated carriers will recombine during their long journey.

Some methods can be employed to minimize carrier diffusion length, i.e. the wafer can be ground to be thinner. Even so, the wafer thickness will be more than 100 microns, which is still too great compared with the diffusion depth.

Another technique is to apply a high reverse bias. However, there are disadvantages with the bias. A high voltage is required to deplete the whole bulk. In practice, 50 - 100V is needed to deplete a wafer a few hundred microns thick, even for the lowest-doped substrate. In addition, an external reverse bias complicates the electronics. Finally, cross-talking may become significant because light-generated carriers at a pixel’s border region may travel to neighbouring pixels.

3 The concept of the novel CT detector micro-module

In this chapter, the working principle of the novel CT detector micro-module is presented. The conceptual verification test results and the assembly process are discussed. The pre-amplification stage circuit configurations and noise performance are discussed. The thermo-mechanical simulation results of the novel detector structure are also presented.

3.1 Working principle of the novel CT detector micro-module

In the novel detector micro-module, photocurrent signals are read out from the bottom side of the photodiode array chip via the silicon bulk. Thus, the problems related to signal routeings, which are discussed earlier, are eliminated. Without signal routeing conductors on the topside of the chip, the light-sensitive surface can cover the full area of the novel micro-module. Thus, it is possible to produce rectangular detector building blocks which contain a number of detector elements. By tiling such building blocks in both directions in a plane, detector array with any number of detector elements (multiple of the number in one building block) can be built. This is the basic principle of the novel detector micro-module.

The cross-section view of the novel micro-module is shown in Fig.28. The top view of the micro-module without the scintillator is shown in Fig.29.

The micro-module shown in Fig.28 and Fig.29 contains 256 (16 x 16) active elements. The scintillator structure is similar to that of the conventional multi-slice CT detector modules. Elements of the photodiode array are physically isolated from each other by dicing. The topside P^+ nodes, which are referred to as anodes in this study, are electrically connected together to ground. The bottom-side N nodes, what are referred to as cathodes in this study, are used as read out nodes. This distinguishes the novel micro-module from the conventional, anode-readout CT detector modules (shown in Fig.21). Each individual cathode node is soldered to a separated pad on the LTCC substrate. Each of the pads is connected to one ball of the BGA (Ball Grid Array) on the backside of the substrate. The BGA makes the connection to the module-level PCB substrate.

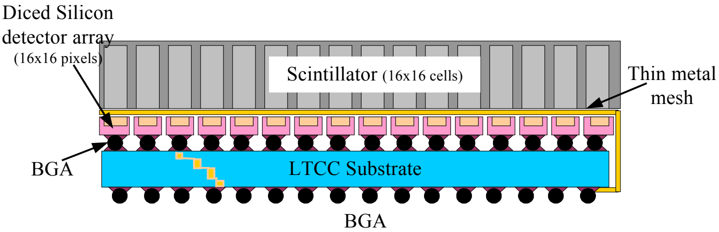


Fig. 28. Cross-section of the novel CT detector micro-module.

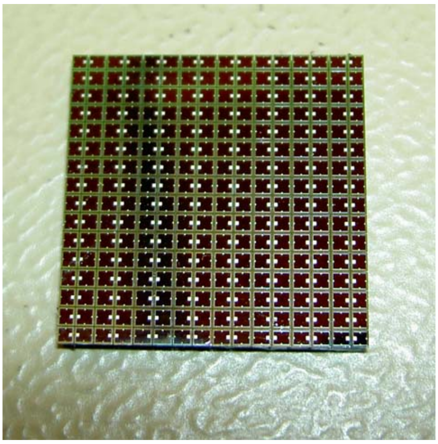


Fig. 29. Top view of the novel CT detector micro-module presented in Fig.28 (without scintillator); The size of the module is approximately 21 x 21 mm^2.

Grounding of the topside anodes is accomplished by soldering every anode pad to a thin metal mesh. The metal mesh has an opening window on the active area of each photodiode pixel. The opening windows let the light emitted by the scintillator enters the detector active area. More details of the metal mesh are discussed in section 4.4.3.

When tiling the micro-modules into modules, the micro-modules are assembled on a PCB by soldering the BGA. The same active element pitch is maintained on z-axis direction. The PCB boards connect the signals from the micro-modules to the system pre-amplification stage either via connectors or flex cables. The PCB boards also serve as the mechanical mounting support for the micro-modules in the gantry.

The term “micro-module” comes from the fact that it is a standard sized “sub-module”, part of a CT detector module.

As an example, a 64-slice CT detector arc can be built by tiling the novel micro-modules in the way shown in Fig.30.

Compared with the conventional CT detector modules, the novel micro-module concept is advantageous in the following respects.

- The detector array is extendable in two directions. Thus CT detector modules with an unlimited number of slices can be built. Detector size is no longer a hindering factor in improving CT system performance.
- Parasitic resistance and capacitance are minimized. Because there is essentially no wiring on the photodiode chip, there is virtually no parasitic resistance or capacitance. As a result, the noise level in the pre-amplification stage is reduced; the noise uniformity among the elements is improved which consequently improves image quality; the response speed is also higher.
- Manufacturing costs are lower. The high-density wire-bonding process is avoided and the production yield can also be improved. Another potential improvement is to make the micro-module to PCB joints by means of re-workable conductive joints, for example, re-workable soldering materials. If some of the pixels in a detector array are damaged, the corresponding detector micro-module can be replaced without replacing the whole detector module.

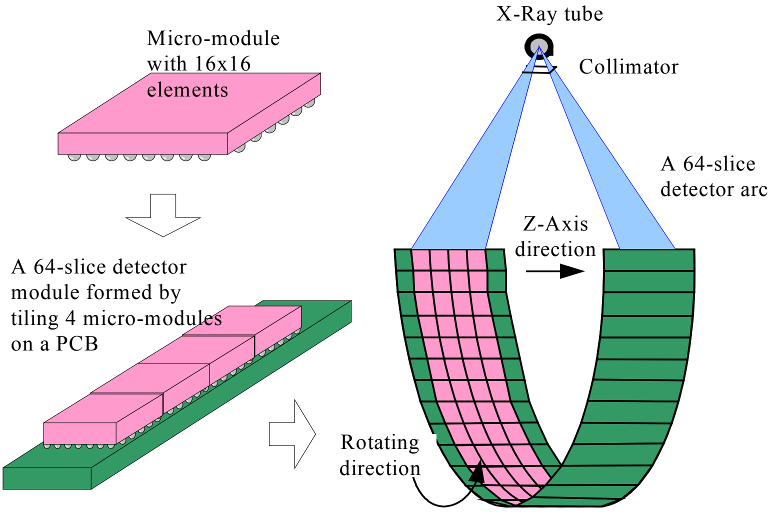


Fig. 30. A 64-slice detector arc built by tiling the novel micro-modules (Not to scale).

Compared with the contemporary next generation solutions proposed by other researchers, the detector micro-module is also advantageous in other respects.

Compared with the flat-panel solution, the photodiode array of the novel micro-module inherits the merits of single-crystal photodiodes. The detector performance is much better than that of the amorphous detector of the flat-panel solution in term of dark current, light sensitivity, response speed and noise level. The manufacturing costs are lower. When the micro-module is assembled to the CT system with re-workable joints, in case of the failure of some detector elements, only the micro-module needs to be removed and replaced. While with the flat-panel detector the whole detector array, which can contain up to a million elements, has to be replaced if the number of the dead elements is not tolerable. The image distortion due to cone-beam illumination can also be alleviated with the novel micro-module.

Compared with the active pixel approach, the photodiode array processing of the novel micro-module is simpler and thus better for the diode performance. The problem caused by open-loop read-out is also avoided.

The back-illuminated detector array is somewhat close to our novel micro-module. However, as analyzed in the previous chapter, in the back-illuminated detector array, the charge collection region is away from the charge generation region. This may cause relatively low absorption efficiency and relatively high cross-talk if no bias is used. If bias voltage is used, the preamplifier electronics becomes more complicated and prone to noise. Such a problem is avoided in our design. In the novel micro-module, we still employ the top surface of the detector as the light sensitive area. The charge generation region, which is close to the top surface, overlaps with the charge collection region, which is the PN junction depletion region. The readout node is on the bottom side of the chip now. But it does not affect the charge collection efficiency. Because once the generated charges start to move, an equivalent current will be generated on the cathode node to maintain the current continuity, no matter how far the node is.

Compared with the conventional CT detector modules, the novel micro-module has two uncertainties. One is, if the dense dicing on small-sized detector elements affects the diode dark current performance. The second is, what is the impact on the pre-amplification electronics when the cathode-readout scheme is adopted.

In the conventional detector array, the pixels in the array are electrically isolated from each other since the signals are read from each of the isolated P regions. However, in the novel micro-module, the signals are readout from the cathode nodes, which is at the same electrical potential for every detector element. To read out the signals separately from each detector element, the array has to be diced into individual elements.

The mechanical stress during dicing causes crystal defects in silicon dies. These defects can become carrier generation-recombination centres. The dark current level of the diode is raised if the density of carrier generation-recombination centres raises. This is why the diode elements on the edges of a diode array usually have higher dark current level than the central ones..

To investigate the dicing effect, a diode array for preliminary test is designed and manufactured. The dark current of diode array is first measured after the diode array is diced off from the wafer. Then the diode array is diced into elements. Each of the elements is bonded to a conductive plane. Then the dark current of each element is then measured again. The typical dark current results at 10mV reverse bias voltage and room temperature before and after dicing are compared in Fig.31.

As shown in Fig.31, after pixel dicing, the dark current is greater, but not dramatically greater than before pixel dicing.

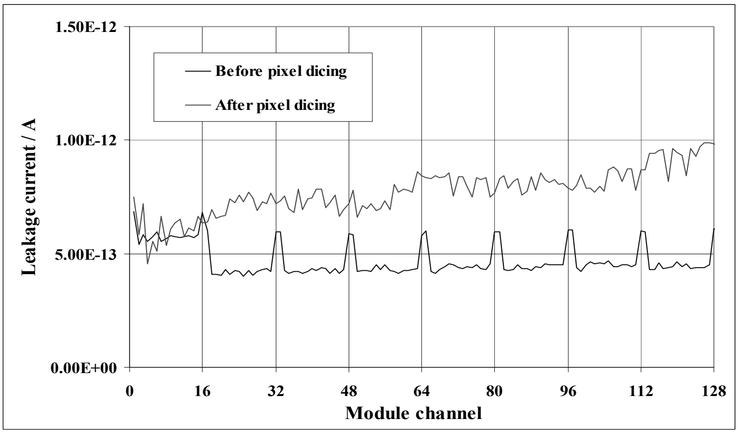


Fig. 31. Comparison of the dark current before and after pixel dicing.

More results regarding the effects of dicing on the novel micro-module photodiodes are reported in Chapter 4.

The electrical circuits of an anode-readout scheme and a cathode-readout scheme are compared in Fig.32.

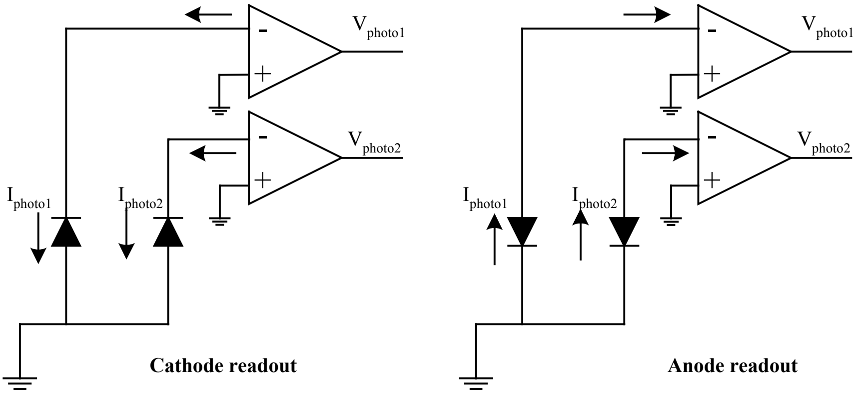


Fig. 32. Comparison of an anode-readout scheme and a cathode-readout scheme.

Obviously, the current polarity of the two schemes is different. This has to be compensated in the pre-amplification stage, as will be discussed later.

The magnitude of the two schemes shall be the same, with both DC signals and AC signals. In a two-node component, the current flow on the two terminals would only be the same if there were no charge accumulation or de-accumulation inside the component.

In other words, if the amount of charge inside the component does not change, then the current flow in and out will be the same. And *vice versa*.

As discussed before, it can be viewed as a capacitor. The accumulated charge inside a photodiode will not change if and only if the voltage drop between its two terminals does not change.

In readout electronics, one terminal of a photodiode is grounded and the other is virtually grounded by the pre-amplification stage, as shown in Fig.32. If the photocurrent is not extraordinarily high, the voltage drop on the photodiode shall be considered as unchanged, neither does the quantity of the accumulated charge. Consequently, the current intensity at the two terminals is the same.

3.2 Front-end electronics analysis

The output current signals of the detector module are connected to the front-end electronics for amplification before they are converted into digital signals. The detector and the front-end electronics are the most crucial parts to achieve the required dynamic range, linearity and imaging uniformity.

There are two types of front-end electronics for X-ray CT applications, the transimpedance amplifier and the switched-capacitor integrator. (Baker 1993)

3.2.1 Transimpedance amplifier

The circuit configuration of the transimpedence amplifier is shown in Fig.33.

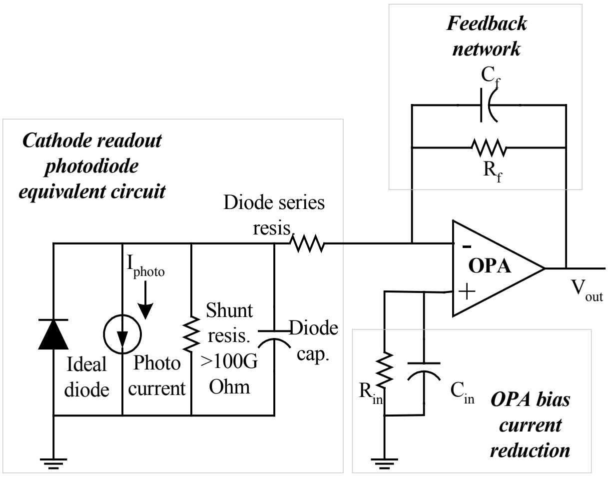


Fig. 33. Equivalent circuit of transimpedance amplifier .

The transfer function of the transimpedenance amplifier is

$$V_{out} = I_{photo} \cdot R_f \cdot (\frac{1}{1+2\pi j\omega R_f C_f}) \qquad (3.1)$$

where the R_f value determines the low frequency gain, and it normally ranges from 10kΩ to 100MΩ depending on the signal level. C_f limits the gain bandwidth with its value normally ranging from sub-pico *pF* to a few *pF* (Baker 1993).
The adoption of the cathode read-out detectors into conventional electronics is easily achieved by omitting the following inverting stage.
There are three noise sources in this circuit configuration; photodiode shot noise, the operational amplifier noise and the thermal noise generated by the feedback network. The noise model of the transimpedance amplifier is shown in Fig.34.

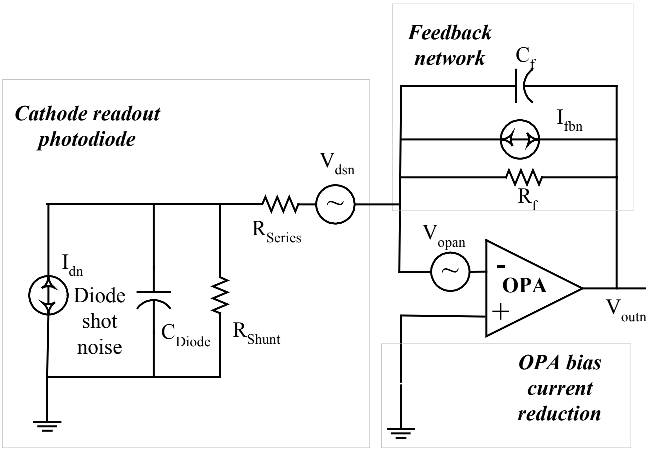


Fig. 34. Noise model of the transimpedance amplifier.

Photodiode noise is dominated by the dark current shot noise I_{dn}. The shunt resistance in the diode electrical model in Fig.34 does not generate thermal noise because it is essentially an equivalent resistor in the small-signal model. The series resistance is normally small, a few ohms to a few hundred ohms. The spectral density function of the dark current shot noise is (Johns & Martin 1996)

$$I_{dn}^{\ 2} = 2qI_{leakage} \qquad (3.2)$$

The typical dark current of one detector element in a CT detector is less than 1E-13A at zero bias and the shot noise spectral density is 3.2E-32A^2/Hz.
The spectral density function of the series resistance is given by (Johns & Martin 1996)

$$V_{dsn}{}^2 = 4kTR_{Series} \tag{3.3}$$

When R_{Series} = 100Ω, the thermal noise PSD generated by the series resistance is 1.65E-18V^2/Hz at room temperature. When R_{Series} = 5Ω, the noise PSD becomes 8.25E-20 V^2/Hz.

The operational amplifier noise can be represented by an equivalent noise voltage source at the input V_{opan}. It is dominated by the thermal noise and flicker noise of the input MOS FET. The noise spectral density functions are given by (Lee *et al.* 2002)

$$V_{opan}{}^2 = V_{thn}{}^2 + V_{fn}{}^2 = \frac{8}{3}\cdot\frac{kT}{g_m} + \frac{K_f}{C_{ox}WL}\frac{1}{f} \tag{3.4}$$

where V_{thn} represents the thermal noise, V_{fn} represents the flicker noise, g_m is the transconductance of the input FET, $C_{ox}$is the gate oxide capacitance per unit area, W and L are the gate width and length of the input FET respectively, K_f is the flicker noise coefficient which depends on the technology (Razavi 2000). The input current noise is ignored in this study because usually an MOS amplifier, with negligible input current, is employed in the readout electronics.

When T = 300K, g_m=10mS, the thermal noise spectral density $V_{thn}{}^2$ = 1.1 x $10^{-18}V^2$/Hz. When K_f = 1x $10^{-25}V^2F$ (Razavi 2000), C_{ox} =2.03fF/μm^2 (Austria Micro System, 1999), WL = 2000μm^2, the flicker noise spectral density at 1kHz is 2.5 x $10^{-17}V^2$/Hz. At 100KHz, it is 2.5 x $10^{-19}V^2$/Hz.

The feedback network contains an *RC* network in which the resistor has thermal noise. The capacitor is noise-free itself, but it accumulates noise from the resistor and contributes a noise proportional to *kT/q* (Razavi 2000). The noise of the feedback network can be represented by a parallel equivalent noise current source I_{fbn}.

$$I_{fbn}{}^2 = \frac{4kT}{R_f} \tag{3.5}$$

When R_f = 10MΩ, T = 300K, the noise spectral density $I_{fbn}{}^2$ = 1.66E-29A^2/Hz.

Applying superposition law and assuming R_{Series} to be negligible compared to R_{Shunt}, the total output noise spectral density function is given by

$$V_{outn}{}^2(f) = [I_{dn}{}^2 + I_{fbn}{}^2]\left|\frac{R_f}{1+j2\pi fR_fC_f}\right|^2 + [V_{opan}{}^2(f) + V_{dsn}{}^2][1+\frac{R_f}{R_{Shunt}}\cdot \left(\frac{j2\pi fR_{shunt}(C_{Diode}+C_{FETIn})+1}{j2\pi fR_fC_f+1}\right)] \tag{3.6}$$

where C_{FETIn} is the input FET capacitance. C_{FETIn} and C_{Diode} together comprise the input capacitance of the OPA.

$$C_{FETIn} = C_{gs} + C_{ov} = \frac{2}{3}WLC_{ox} + WC_{gsdo} \tag{3.7}$$

where C_{gs} is the gate to substrate capacitance, C_{ov} is the overlap capacitance between the substrate and the source, C_{ox} is the gate capacitance per unit area, C_{gsdo} is the gate to source or drain overlap capacitance per unit distance. C_{gox} and C_{gsdo} depend on the process technology. If a commercial 0.8μm process is used where WL= 2000μm^2 then C_{FETIn} is about 4pF. C_{Diode} is usually 15 to 30pF in a conventional CT detector module and about 10pF in the novel micro-module. C_{Diode} is the main component of the input capacitance.

When considering the above estimated typical values of I_{dn}^2, I_{fbn}^2, $V_{opan}^{\ 2}$and V_{dn}^2, we come to the following conclusions.

First, the dark current shot noise I_{dn}^2 is negligible compared to the feedback resistor thermal noise. As will be presented later, the dark current of the novel micro-module after pixel-dicing (see Chapter 5.) is approximately doubled. However, according to the above analysis, the higher dark current will have little effects on the system level performance.

Second, when the diode series resistance is 100Ω, its thermal noise is not negligible especially at a relatively high frequency, but when the resistance is around 5Ω, it is negligible over the whole signal bandwidth. As will be discussed later, the series resistance of the middle detector pixels in a conventional CT detector module is more than 100Ω due to the long wiring. In the novel micro-module, the detector series resistance is around 5Ω in all pixels.

At low frequency equation (4.7) can be simplified into equation (3.8).

$$V_{outn-low}^{\ \ 2}(f) \approx I_{fbn}^{\ 2} R_f^{\ 2} + [V_{dsn}^{\ 2} + V_{opan}^{\ \ 2}(f)](1 + \frac{R_f}{R_{Shunt}}) \tag{3.8}$$

Considering the previously calculated typical values, this can be further simplified into (3.9).

$$V_{outn-low}^{\ \ 2}(f) \approx I_{fbn}^{\ 2} R_f^{\ 2} \tag{3.9}$$

At low frequency, the thermal noise of the feedback network dominates. However, the noise bandwidth for this noise is very limited. It is given by (3.10) (Razavi 2000)

$$f_{fbn} = \frac{\pi}{2} \cdot \frac{1}{2\pi R_f C_f} = \frac{1}{4R_f C_f} \tag{3.10}$$

When R_f = 10MΩ and C_f = 10pF then f_{fbn} = 2.5KHz.

At high frequency, equation (4.7) can be simplified into equation (3.11)

$$V_{outn-high}^{\ \ 2}(f) = [V_{dsn}^{\ 2} + V_{opan}^{\ \ 2}(f)](1 + \frac{C_{Diode} + C_{FETIn}}{C_f}) \tag{3.11}$$

The total noise power spectral density of the transimpedance circuit is shown in Fig.35. The decline at high frequency is due to the open-loop gain bandwidth roll off of the operational amplifier.

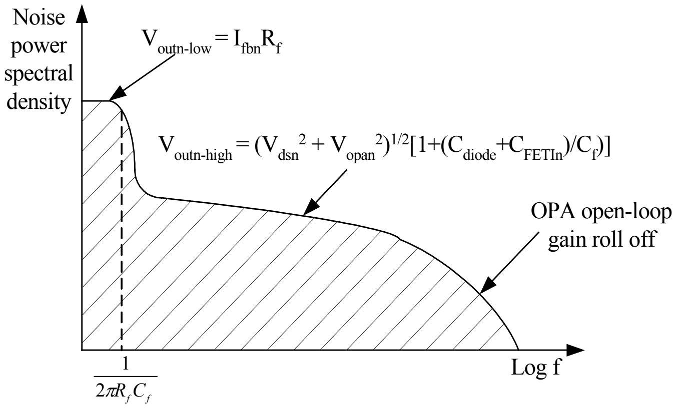


Fig. 35. Noise spectrum of the transimpedance circuit.

The noise in time domain is equal to the integral of the above spectrum curve, i.e. the shaded area in Fig.35. The OPA noise gained by $1+(C_{diode}+C_{FETIn})/C_f$ is the most significant part. By decreasing C_{diode}, the overall noise performance of the transimpedance amplifier can be decreased proportionally. As will be discussed later, the capacitance of the novel detector micro-module is only 50% of that of the conventional detector modules because the wiring parasitic capacitance is absent.

3.2.2 Switched-capacitor Integrator

The equivalent circuit configuration of a switched-capacitor integrator, or say, a charge sensitive amplifier is shown in Fig.36.

The basic operation principle is as follows. In the reset phase, S_1 is first opened to isolate the OPA input from the diode output. S_2 is closed to reset. Then integration phase follows, S_1 is closed and S_s is opened. Light-generated current flows away from C_f, causing a voltage rise at V_{out}.

$$V_{out} = \int_0^T \frac{I_{Photo}}{C_f} dt \tag{3.12}$$

where T is the integration period. Compared with the conventional anode-readout application, the voltage polarity is reversed.

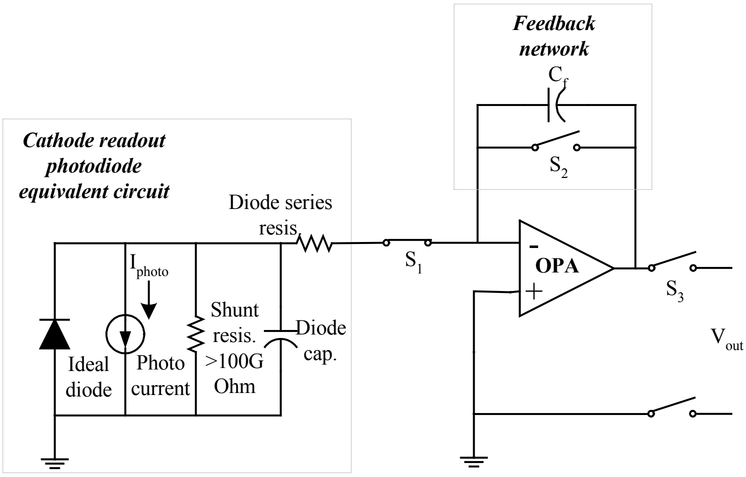


Fig. 36. Circuit configuration of a switched-capacitor integrator with photodiode equivalent circuit .

The noise model of the integrator is shown in Fig.37.

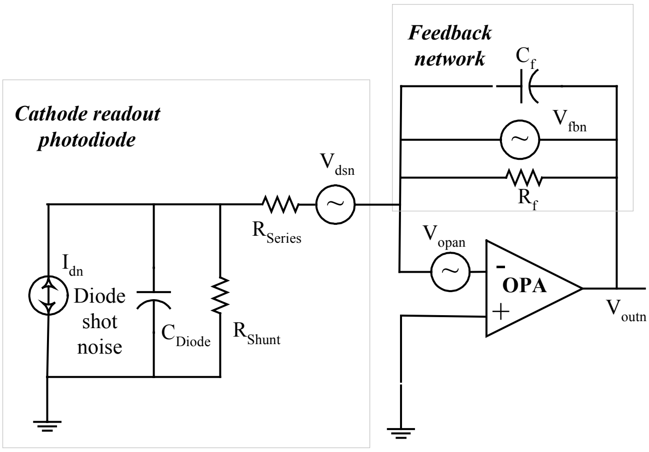


Fig. 37. Noise model of the switched-capacitor integrator.

The photodiode noise and the operational amplifier noise analysis is similar to that of transimpedance configuration.

In the feedback network, R_f is the equivalent open resistance of the switch S_2, and can be deemed to be noise-free since it is an equivalent resistor. Its value is normally in the order of 1000GΩ (Baker 1993). The feedback noise source V_{fbn} is dominated by the capacitor kT/C noise. It is given by (Johns & Martin 1996)

$$\int_0^\infty V_{fbn}(f)^2\,df = \frac{kT}{C_f} \tag{3.13}$$

The value of C_f can be from more than 10 pf up to more than 100pf. V_{fbn} is in the order of some μ V at the output. This would be a very significant noise for the CT system if it cannot be removed. However, the kT/C noise is only within the bandwidth of the R_fC_f network, which is at very low frequency, usually sub-Hz. With switched-capacitor approach, the low frequency noise can be easily removed by using CDS (Correlated Double Sampling) technique. (Wang 2002)

The total noise power spectral density is given by

$$\begin{aligned} V_{outn}{}^2(f) = {} & I_{dn}{}^2\left|\frac{R_f}{1+j2\pi f R_f C_f}\right|^2 + [V_{opan}{}^2(f)+V_{dsn}{}^2][1+\frac{R_f}{R_{Shunt}}\cdot(\frac{j2\pi f R_{shunt}(C_{Diode}+C_{FETIn})+1}{j2\pi f R_f C_f+1})] \\ & +\frac{kT}{C_f\cdot BW_{noise}} \end{aligned} \tag{3.14}$$

where BW_{noise} is the noise bandwidth determined by R_fC_f.

At low frequency, (3.14) can be simplified by

$$V_{outn-low}{}^2(f) = I_{dn}{}^2R_f{}^2+[V_{opan}{}^2(f)+V_{dsn}{}^2](1+\frac{R_f}{R_{Shunt}})+\frac{kT}{C_f\cdot BW_{noise}} \tag{3.15}$$

The magnitude is high because R_f is very high. But as discussed before, the bandwidth is very small. With the CDS technique, the low frequency noise can easily be removed.

At high frequency, (3.14) can be simplified by

$$V_{outn-high}{}^2(f) = [V_{dsn}{}^2+V_{opan}{}^2(f)](1+\frac{C_{Diode}+C_{FETIn}}{C_f}) \tag{3.16}$$

This is similar to the conclusion made with the transimpedance amplifier. The dominating noise factor is the OPA noise gained by the factor of $1+(C_{diode}+C_{FETIn})/C_f$. By using the novel detector micro-module, the noise performance should be significantly improved.

3.3 Main assembly steps

An overview of the main assembly steps is briefly discussed in this section. More details of the assembly, Manufacturing of the silicon wafer and LTCC substrate are covered in chapter 4.

The main assembly steps are shown in Fig.38. The silicon wafer is firstly diced into diode arrays. Then the metallization of silicon chips is coated with solderable metal layers. After that the backside of the silicon die is coated with a solder mask layer which leaves one opening for each diode element.

The LTCC substrate is manufactured with the same pad layout as the solder mask openings on the bottom of the silicon chip. After the pads on the LTCC substrate is coated with solder paste, the silicon chip is attached to the substrate with a fine alignment equipment. After that, the substrate with the attached silicon die is reflowed to make solder joints.

Under-fill material with low viscosity is feed to fill the gap between the silicon die and the substrate. The under-fill provides good mechanical bonding between the silicon die and the substrate. After under-fill, the silicon die is diced into 16 x 16 elements. Fine control of dicing depth is required to fully separate the silicon bulk and at the same time not to dice into the substrate.

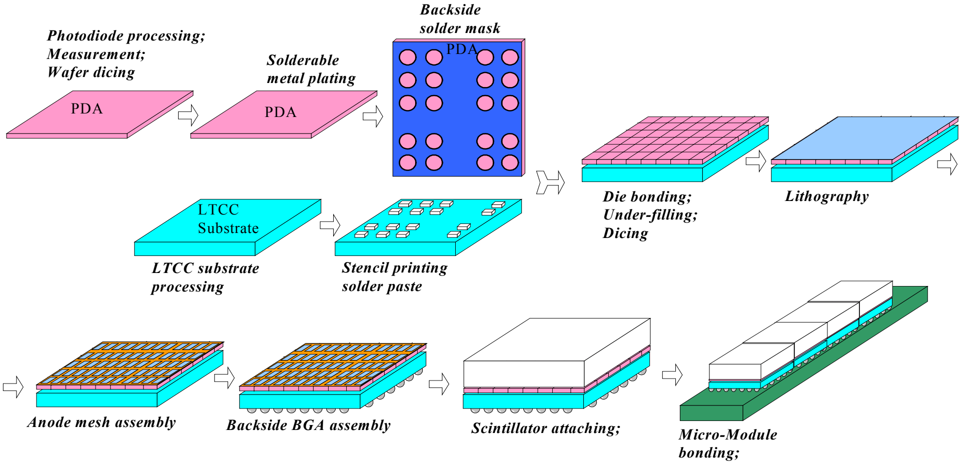


Fig. 38. Main steps in assembling the novel detector micro-module and tiled detector module.

The top anode connection is done by soldering the P^+ node pads of every element to a thin metal mesh layer. A layer of photoresist is coated to the top surface of the micro-module in order not to contaminate the active surface. A lithography process is used to make openings on anode pads for soldering.

The backside of the substrate has an array of circular pads. Solder paste is dispensed on every pad. Then an array of solder balls are attached to the pad array. The whole module is reflowed to make the BGA.

The gap between the scintillator and the silicon die is filled with a transparent epoxy material which optically coupled the scintillator to the silicon detector. Special care is taken to avoid air-bubbles left inside the epoxy.

3.4 Thermo-mechanical simulation

To ensure that there is no high thermo-stress due to the relatively complicated assembly process and the high-temperature assembly steps, thermo-mechanical simulation of the micro-module structure was performed with the finite element analysis program Ansys.

An overview of modeling and simulation work and the main conclusions are discussed in this section. More details of the simulation work are presented in Appendix III.

Due to the complexity of the module structure, the simulation was divided into three phases. Each phase represents an actual high-temperature assembly process, i.e. die-bonding, top anode connection and module assembly. An individual geometry model was established for each phase and addressed to determine the stress caused by the corresponding assembly process. The geometry models were simplified by ignoring the components irrelevant to the specific process.

In phase 1, the stress field during die-bonding process was studied. There are two approaches to do die-bonding. One is to have a solder ball on each pad to maintain the distance between the silicon die and the LTCC substrate. This is referred to as ball-die-bonding in this study. The other way is to direct bond the silicon die to the substrate with a layer of solder paste between them. This is referred to as direct-die-bonding in this study. The geometry models of both approaches are shown in Fig.39. The details of the photodiode structure were omitted in the simulation.

The simulation in phase 1 shows the ball-die-bonding has lower mean stress than direct-die-bonding.

In phase 2, thermal-mechanical stress after anode connection was studied. The geometry model in phase 2 is shown in Fig.40. In this phase, the photodiode array has been diced into individual pixels. To simplify the simulation, the residual stress from die-bonding was considered to be released prior to phase 2.

In phase 3, thermal-mechanical stress raised by soldering between the micro-module and the module-level PCB was studied. The rest of the structure was omitted. The geometry model is shown in Fig.41.

In all the simulations, the model was deemed to be stress-free at the melt point temperature of the solder material.

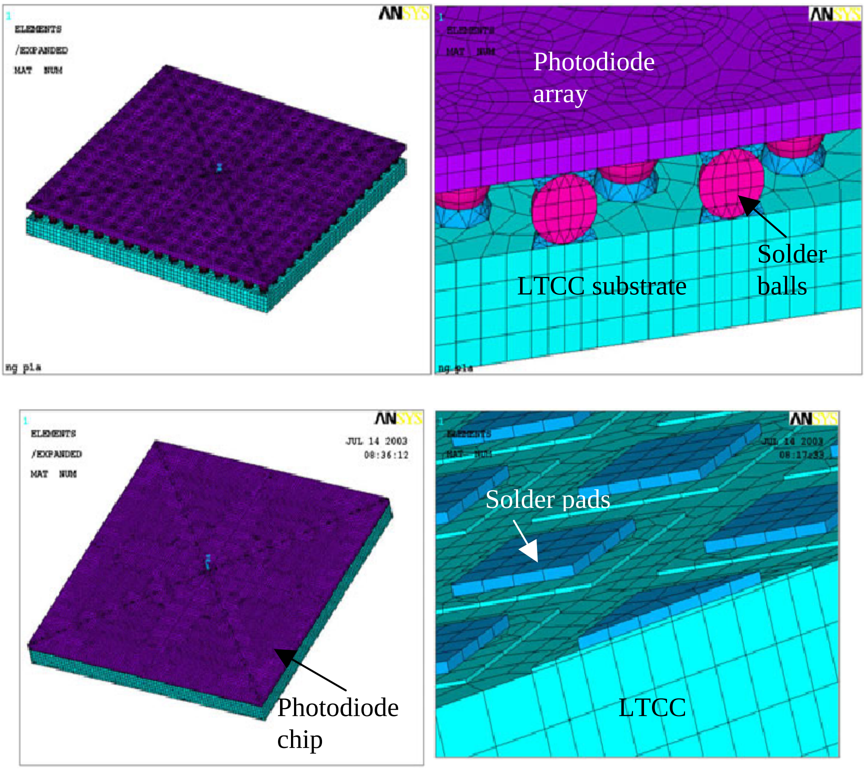
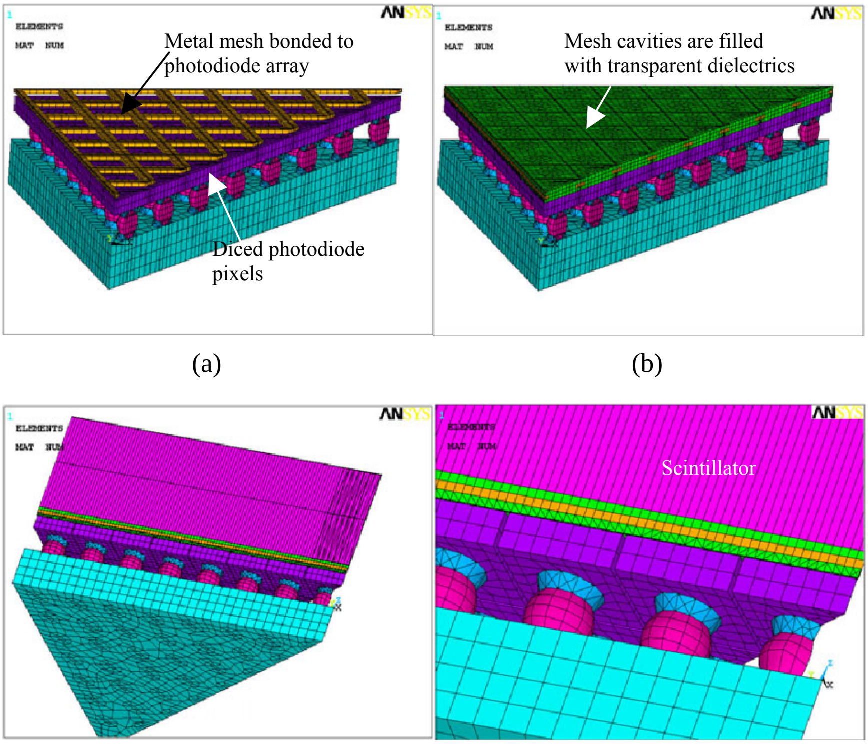


Fig. 39. Geometry models of the novel detector micro-module for the 1st phase thermal stress modeling and simulation; Upper two figures: Geometry model for ball bonding approach in phase 1 die-bonding simulation,; Lower two figures: Geometry model for direct bonding approach in phase 1 die-bonding simulation, on the left side is the overview of the model, on the right side is the enlarged cross-section view.

Due to the difficulty in acquiring the material parameters, we assume all materials are linear, i.e. that there was only elastic stress. The 2nd order effects, such as plasticity and creeping, were not considered here. Solidification of the solder fluid was considered to occur instantly without delay. Because in reality most of the stress would be released during cooling-down and this could not be simulated, we assumed the residual stress was 25% of the full stress.

Because of the simplifications made, it is doubtful how well the simulation results match with reality. To make the simulation results more reliable, we simulated the thermal-mechanical stress of a typical present-generation CT detector module with all the same assumptions. By comparing the simulated residual stress from the two modules, we could estimate whether the novel micro-module experience extraordinarily high thermal stress during the assembly compared with the mature present-generation products. This was the main purpose of the simulation.



(a) (b)

(c) (d)

Fig. 40. Geometry model for the 2nd phase simulation; (a) Diced photodiode array assembled with metal mesh; (b) Gaps in the metal mesh are filled with transparent dielectric material; (c) Overview of the full geometry model, Scintillator has been attached; (d) Zoomed view showing the structure.

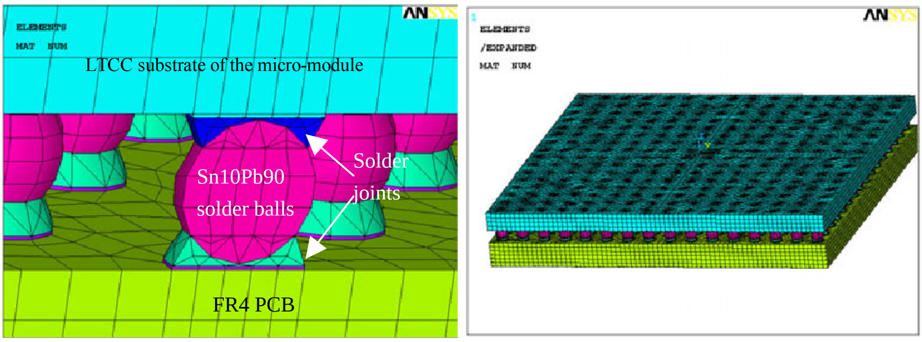


Fig. 41. .Geometry model of the 3rd phase simulation, Left: overview; Right: enlarged view.

The simulated distribution of the residual stress is shown in Fig.42. The numerical values of the residual stresses on silicon chips are shown in Table 2. For the Present-G modules, the stress is simulated for temperature variations from 25°C to 120°C, assuming the curing temperature of the conductive epoxy is 120°C. The stress of the novel micro module is simulated for temperature variations from 25°C to 180°C, which is the melting temperature of the SnPb solder.

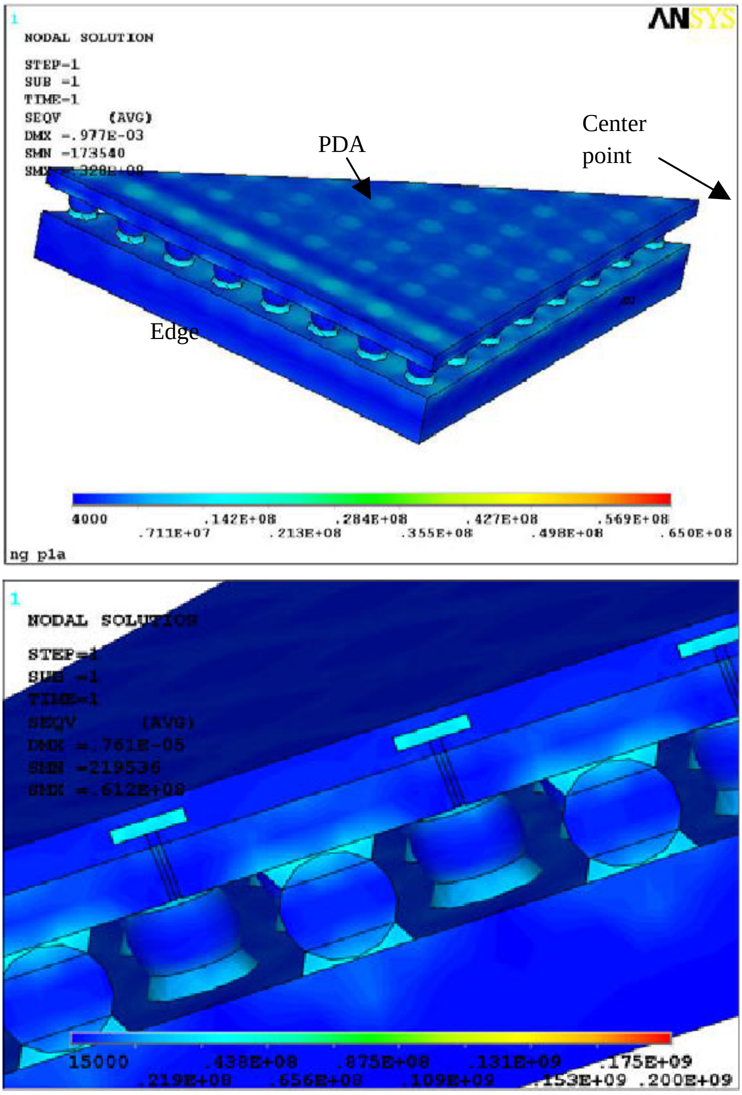


Fig. 42. The simulated residual XY shear stress distribution in the module (Unit: Pa); the red color represents high stress. Upper: 1/8 of the module; Lower: Enlarged cross-section view.

Table 3. Simulated residual XY shear stress on silicon chip after assembly.

Module	Stress [MPa]		
	Minimum	Maximum	Mean (over elements)
Present-G. Module	0.4	20.0	11.1
Micro-module, ball-die-bonding	0.3	32.3	7.1
Micro-module, direct-die-bonding	0.1	27.3	8.2

The maximum and minimum values shown in Table 3 only reflect the range of the stress. They should not be used as the criteria in comparing the three structures. This is because they were highly dependent on the assumptions made and thus do not necessarily reflect the reality. Also, non-convergence and numerical instability will also affect the maximum and minimum value.

The mean value is likely to be closer to the reality, so the conclusion may be made that the micro-module with ball-die-bonding structure experiences the least stress in assembly. And the mean stress is less than or on the same level as that of the conventional module assembly process.

The stress caused by the temperature variation during transportation and operation is insignificant compared with that undergone during assembly.

4 Realization of the novel detector micro-module

In this chapter, the design and the manufacture of the novel detector micro-module are presented and discussed. The photodiode array for the novel detector micro-module is discussed, including its design, processing and characterization measurement results. The photodiode array measurement results are compared with a typical multi-slice CT detector module photodiode array for benchmarking. The design, manufacture and characterization measurement results of the multi-layer LTCC substrate are presented. The assembly process of the novel detector micro-module is reported and discussed. Test results of the detector array after each main assembly step are monitored and reported.

4.1 Photodiode array

4.1.1 Design of the photodiode array

The layout of the photodiode array for the novel micro-module is shown in Fig.43. The cross-section of one pixel in the array is shown in Fig.44.

The pixel pitch is designed to be approximately 1.4 x 1.4mm^2. However, it can be made smaller. The minimum size of the detector element in the novel micro-module is determined by the minimum space required for dicing, because the dicing edge must be kept far enough away from the active area to avoid the possibile mechanical damage. In this study, a 250µm space between active areas is used. To determine the minimum safe space, further investigation is needed.

The size of detector elements on the edges of the array is a bit smaller than that the middle elements in order to leave a margin for mechanical tolerance in the following assembly processes.

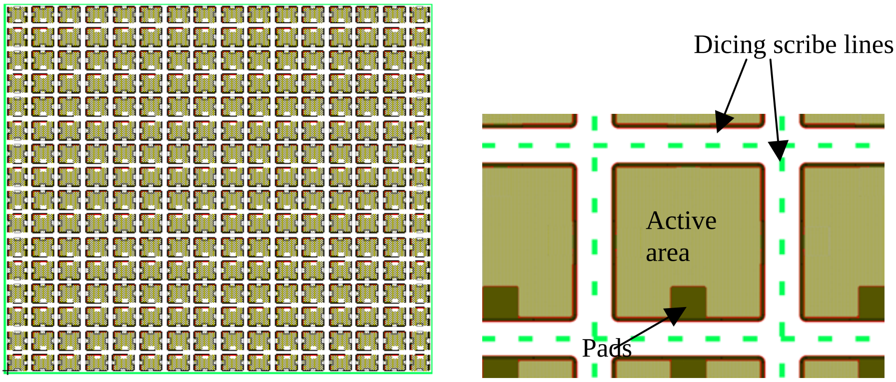


Fig. 43. Layout of the photodiode array for the novel detector micro-module, Left: top view of the whole array; Right: enlarged top view of one pixel.

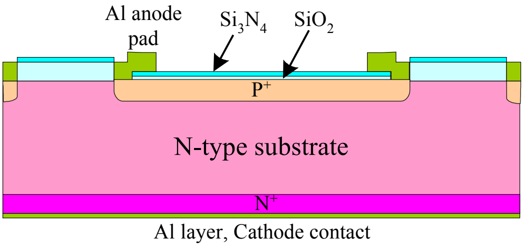


Fig. 44. Cross-section view of one photodiode pixel in a photodiode array for the novel detector micro-module.

4.1.2 PDA Processing

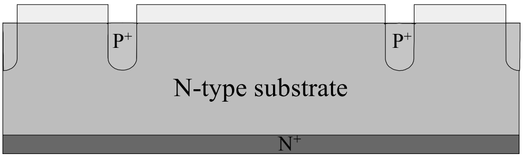
Four lithography photo-masks are needed to manufacture the structure shown in Fig.44. The processing steps are shown in Fig.45. The PDA processes are made in Detection Technology's detector manufacturing facility in Hongkong.

To realize the depletion region with reasonable width, high resistivity N-type wafers are used for photodiode manufacturing. The resistivity is around a few hundred Ohm·cm, which corresponds to a doping density of about $5x10^{14}$ cm^{-3}.

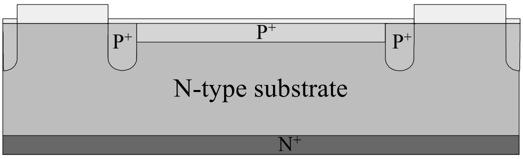
A thick thermal oxide layer is first grown on the wafer. Then Lithography 1 is applied to open the windows on the ohmic contact area. High-energy boron implantation is applied to the top surface. After the subsequent drive-in process a highly-doped deep P^+ ring if formed around the active area. This ring is for the ohmic contact of the active area (the anode node of the photodiode). The thickness of the doped layer is about 2um. The backside of the wafer is then implanted with high-dose phosphorus, which will later form the backside ohmic contact for the cathode node.

Lithography 2 is then applied to open the active area. Firstly, the thick oxide layer above the active area is removed. Secondly, a thin SiO_2 layer is grown as the implantation protection layer. Thirdly, the active area implantation follows and forms the thin P^+ region. The implantation energy, dose and annealing temperature are optimized for visible light detection. The final junction depth is about 0.5 – 1um. The peak doping density is in the order of 10^{16} – 10^{17} cm^{-3}. After annealing, the protection layer is removed. A new thin oxide layer is grown followed by the Si_3N_4 anti-reflection layer growth. The quality of the oxide layer is crucial for the diode dark current level and its short wavelength sensitivity. Special treatments are required here.

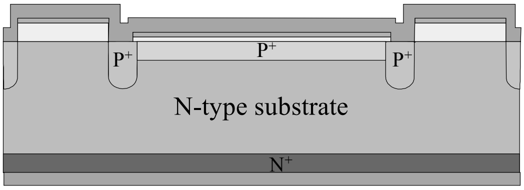
Lithography 3 opens the metallization contact holes. A layer of aluminium is then sputtered on both the top and the bottom layers of the wafer. Lithography 4 is applied and the extra aluminium is removed leaving only the routeings. The wafer is then alloyed to form the ohmic contact.



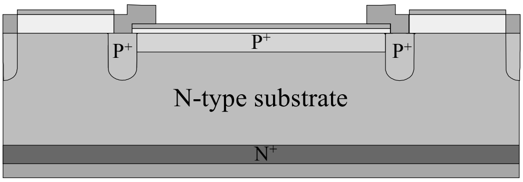
Lithography 1, ohmic area implantation



Lithography 2, active area implantation



Lithography 3, contact hole opening



Lithography 4, Al etching

Fig. 45. The processing steps of the photodiode array for the novel detector micro-module.

The phosphorus implantation on the backside of the wafer also has the effect of reducing the diode dark current (Betta *et al.* 1997). The techniques of oxidation, annealing and alloying reported by H. Wang in his doctoral thesis are employed here to achieve good dark current performance. (Wang 2001) The special cleaning process that was proposed by Kafai Lai *et al.* is also adopted in the processing to further reduce the surface state dark current. (Lai *et al.* 1994)

Compared with conventional CT detector processing, an important improvement is that no thick passivation oxide layer is needed in the novel micro-module photodiode array. In conventional CT detector processing, a thick layer of SiO_2 is required to reduce the routeing parasitic capacitance between signal lines and the substrate. Since there is essentially no signal routeing in the novel micro-module photodiode array, the thick oxide layer is not necessary. This offers the possibility of improving the light absorption by using a thin anti-reflection layer of Si_3N_4. The spectral response measurement results are presented and discussed in the following section.

4.1.3 Photodiode array characteristic measurement results

4.1.3.1 Dark current

The dark current is measured at 10 mV reverse bias at 25 °C. A typical measurement result of a photodiode array is shown in Fig.46. This result was measured from a photodiode array after it was diced off from the wafer. The rise of the dark current seen on the edges of the photodiode array is due to the dicing effects, as discussed previously.

The typical value for a middle pixel is less than 4×10^{-13}A, which corresponds to less than 30pA/cm^2. It is significantly improved compared to the level of 80pA/cm^2, which H. Wang reported as the lowest at that time (Wang 2001).

As a comparison to the measured results, the dark current density is also theoretically calculated using the equation (2.9). In equation (2.9), because normally the doping density in P^+ region is much higher than that in the N region, the dark current is mainly determined by the second term which is the dark current generated in N region. Therefore equation (2.9) can be simplified as

$$J_s \approx \frac{qD_p p_{n0}}{L_p} = q\left(\frac{D_p}{\tau_p}\right)^{1/2} \frac{n_i^2}{N_d} \tag{4.1}$$

where D_p, τ_p, L_p are the diffusion coefficient, minority carrier lifetime and diffusion length of holes in N region; p_{n0} is hole density in the N region at equilibrium; n_i is the carrier density in intrinsic silicon; N_d is the doping density in the N region.

Using τ_p = 0.35ms (Okmetic Ltd 2004), $N_d = 1 \times 10^{14}$/cm^3, D_p = 50 cm^2/s (Sze 2002, page 51) and $n_i = 9.65 \times 10^9$/cm^3, the dark current density is about 5.2pA/cm^2.

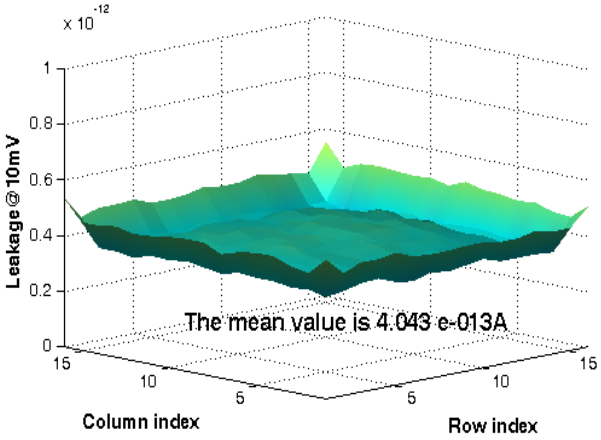


Fig. 46. Dark current results of a typical photodiode array for novel detector micro-module, measured from the photodiode array before diced into pixels.

The result is close to, but not in full agreement with the measured result. There are many reasons for this. The main reasons are the followings; (i.) The minority carrier lifetimes used in the calculation are those for the un-processed pure wafer. The photodiode processes, especially the doping processes degrade the perfection of the wafer and contribute to a higher density of recombination centres. Therefore the minority carrier lifetime becomes shorter and the dark current higher; (ii.) The theoretical calculation assumes the junction is in the bulk. However, in reality, the junction depletion region will partly extend to the surface of the silicon bulk where the Si-SiO2 interface energy states can also become recombination centres and will therefore contribute to the dark current; (iii.) The moisture on the top surface of the SiO2 layer and on the sidewall of the diced photodiode chips can also form a weak electrical path between the anode and the cathode and hence, when there is a potential difference, contributes another type of dark current.

4.1.3.2 Spectral response

Spectral response measurements are made with single packaged photodiodes 2.5mm x 2.5mm in size. These diodes are produced on the same wafer as the PDAs for the novel detector micro-module. Therefore their light response shall be very close to the PDA for the novel detector micro-module.

The details of the measurement system are presented in Appendix II. In short, the photodiode under test is exposed to an incident light beam whose focal point is adjusted to be inside the photodiode active area. The wavelength of the incident light sweeps from 320nm to 1040nm with a step of 20nm. The photocurrent output from the photodiode is

measured at every wavelength step. The incident light intensity is measured with a calibrated photodiode. Then the light sensitivity is calculated using equation (2.7).
A typical spectral response curve measured at 25 °C is shown in Fig.47. As a comparison, the theoretical sensitivity assuming 100% quantum efficiency, and the typical spectral response of a conventional CT detector photodiode in the same size are also shown in the same figure. The numerical values of the corresponding curves are given in Appendix V.

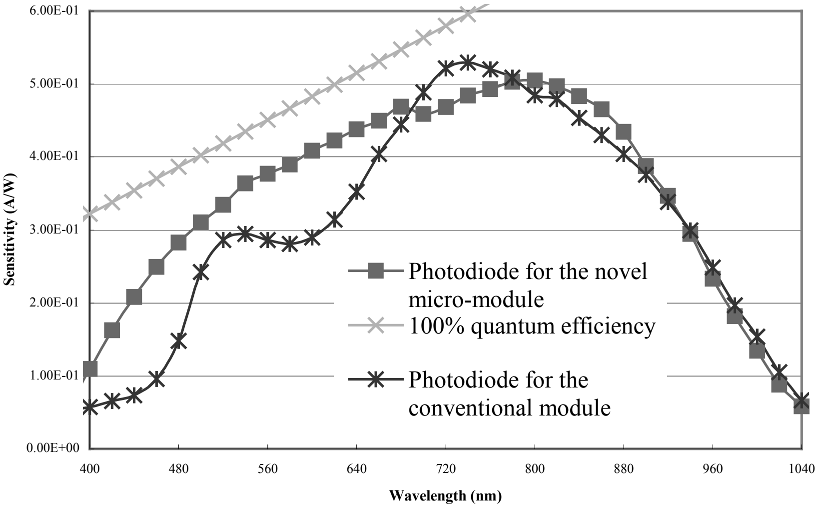


Fig. 47. Spectral response measurement results of the novel micro-module PDA compared with that of conventional CT detector PDA and the sensitivity corresponding to 100% quantum efficiency.

With the optimized doping profile, the photodiode for the novel micro-module shows excellent sensitivity in the wavelength range from 500nm to 660nm. The peak quantum efficiency is calculated, from equation (2.8), to be nearly 90% at 720nm. At the normal scintillator emission wavelengths, from 500nm to 550nm, the quantum efficiency is about 60% to 68%.
The measured spectral response of the photodiode for the novel micro-module is better than that for a conventional module in that there is no fluctuation with wavelength. The fluctuation is due to light interference at the passivation oxide layer. As shown in Fig.48, the incident light is reflected at the top surface of the passivation layer as “Reflection 1”. The incident light is also reflected at the interface below the passivation layer, as “Reflection 2”.

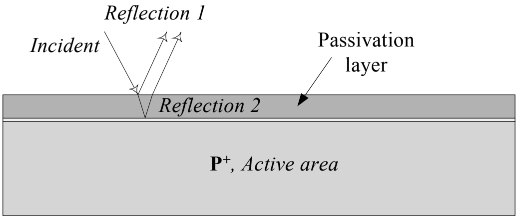


Fig. 48. Interference in the PDA for conventional detector modules.

When the thickness of the passivation layer d satisfies equation

$$2d = k\lambda_n + \frac{1}{2}\lambda_n \qquad (k = 1,2,3..... \quad) \qquad (4.2)$$

Reflection 1 and reflection 2 are of opposite phase (assuming the refractive index of the passivation material is greater than that of the incidence media and less than that of silicon), destructive interference occurs and the total reflection is reduced. Thus, a peak in the sensitivity curve is observed.
where λ_n is the incident wavelength in the passivation material and is given by

$$\lambda_n = \frac{\lambda}{n} \qquad (4.3)$$

where λ is the wavelength in vacuum and n is the refractive index of the passivation material.
When the thickness of the passivation layer d satisfies the equation

$$2d = k\lambda_n \qquad (k = 1,2,3..... \quad) \qquad (4.4)$$

reflection 1 and reflection 2 are of the same phase (assuming the refractive index of the passivation material is greater than that of the incidence media and less than that of silicon), constructive interference occurs and the total reflection is enhanced. Thus, a valley in the sensitivity curve is observed.
In conventional CT detectors, the passivation layer thickness is around 800 – 1200nm. It raises multiple interference peaks and valleys in the sensitivity curve, as shown in Fig.4.5. For example, when the oxide layer thickness is 900nm, using equation (4.4), it is easy to determine that there are three absorption valleys in the wavelength range shown in Fig.4.5. They are at λ_n = 327, 400 and 514nm, corresponding to vacuum wavelength of 474, 580 and 745nm respectively, assuming that the refractive index of SiO_2 is 1.45. This fluctuation has a negative effect on CT imaging. Due to the processing variation, the passivation oxide thickness can change from wafer to wafer and from batch to batch. When PDAs from different wafers and different batches are placed in the same system, a non-uniform response at a given wavelength results. This has to be corrected at system level at the expense of the dynamic range or noise performance.

Since a passivation layer is not needed in the PDA for the novel micro-module, a thin Si_3N_4 anti-reflection layer can be used instead. The layer thickness is around 100nm in the diodes developed in this thesis. Because the anti-reflection layer is thin, it will raise only one absorption peak in the wavelengths of interest, therefore the fluctuations in the sensitivity curves are avoided. For example, when the oxide thickness is 100nm, with equation (4.4) it can be shown that there is only one interference peak at λ_n = 200nm in Si_3N_4, which corresponds to a 400nm wavelength in vacuum space. According to equation (4.2), there is no absorption valley within the wavelengths of interest.

4.1.3.3 Forward I-V characteristics, diode resistance and capacitance

The forward I-V characteristics and the diode series resistance were measured with an HP 4165 semiconductor parameter analyzer. In the measurement, a sweeping forward voltage source was applied to the diode until the forward current was greater than 100mA or the applied voltage was higher than 2V. The forward-biased I-V characteristic is plotted. The inversed slope after threshold is calculated as the dynamic resistance R_{Dyn}, shown in Fig.49. In Fig.49, the X-axis is the forward bias voltage. Because the voltage is applied to the N node of the diode, the voltage is negative. The Y-axis is the measured forward current.

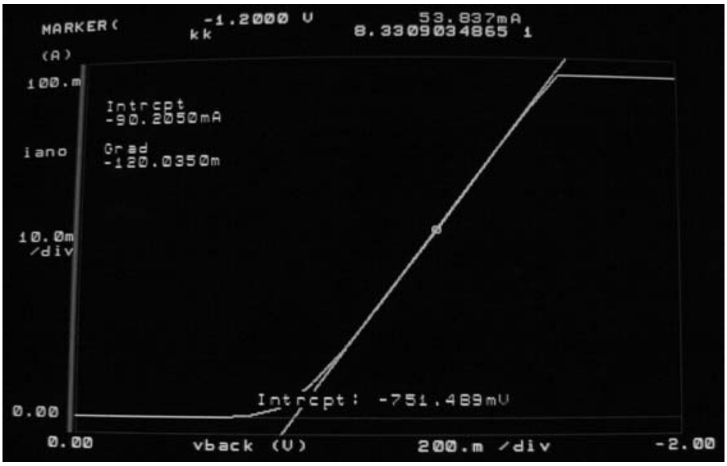


Fig. 49. Measurement of the forward I-V curve and the diode series resistance.

However, to be exact, the measured dynamic resistance R_{Dyn} differs from the series resistance R_{Series} although they are closely related. In a practical diode with series resistance, the equivalent electrical symbol is shown in Fig. 33. The forward bias voltage V and forward current I satisfy the equation

$$I = I_0 \exp\left[\frac{q(V - IR_{Series})}{kT}\right] \tag{4.5}$$

The series resistance can be deduced from the equation

$$R_{Series} = \frac{\partial V}{\partial I} - \frac{kT}{qI} = R_{Dyn} - \frac{kT}{qI} \tag{4.6}$$

where V is the forward bias voltage; I is the forward current; k is Planck's constant; T is the temperature; q is the electron charge; R_{Dyn} is the dynamic resistance measured in the way described previously.

In the measurement, I is usually about 50mA. At room temperature, kT/q is 26mV. Thus, in equation (4.6), R_{Dyn} is usally much greater than the second term. In this thesis, the measured R_{Dyn} is directly used as the series resistance.

The typical resistance of a PDA for the novel micro-module is shown in Fig.50. The typical resistance for a PDA for a conventional detector module is shown in Fig.51.

The series resistance of the micro-module PDA is much smaller than that of the PDA for a conventional CT module. This is because there is almost no wiring parasitic resistance in the novel micro-module PDA. The PDA for a conventional detector module shows a much higher series resistance in central pixels than in the edge pixels.

The diode capacitance is measured with a diode C-V analyzer. The capacitance is measured at zero DC bias, 100kHz signal frequency. In order to make the comparison more convenient to compare, typical measurement results of a PDA for the novel detector micro-module and for a commercial multi-slice CT detector module are normalized to the pixel area and shown in Fig.52 and Fig.53, respectively.

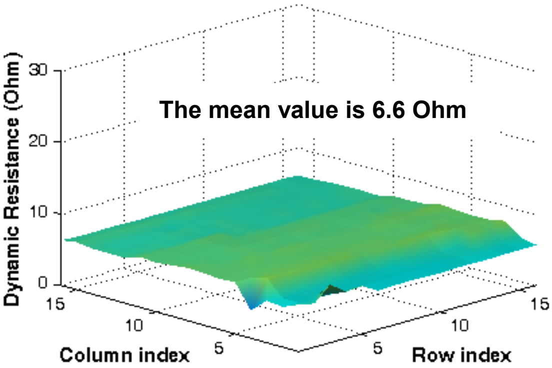


Fig. 50. Typical diode series resistance distribution in a photodiode array for the novel detector micro-module.

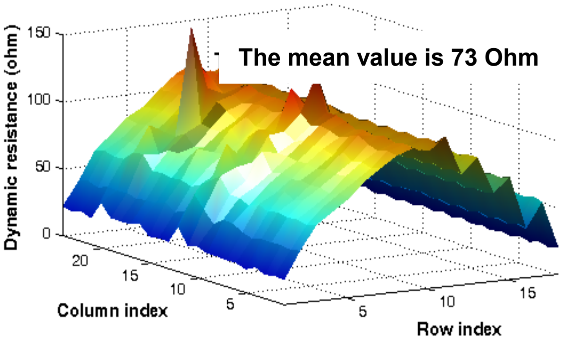


Fig. 51. Typical diode series resistance distribution in a photodiode array for a conventional CT detector module.

Because the two types of photodiode arrays are manufactured on similar types of wafers, their normalized capacitance values should be close. However, the capacitance of the commercial product is much higher than that of the novel micro-module. As discussed before, this indicates that the novel micro-module should have a better noise performance. The capacitance value is uniform in the PDA for the novel micro-module, while in the commercial module the normalized capacitance of the central pixels is almost three times of that of the edge pixels.

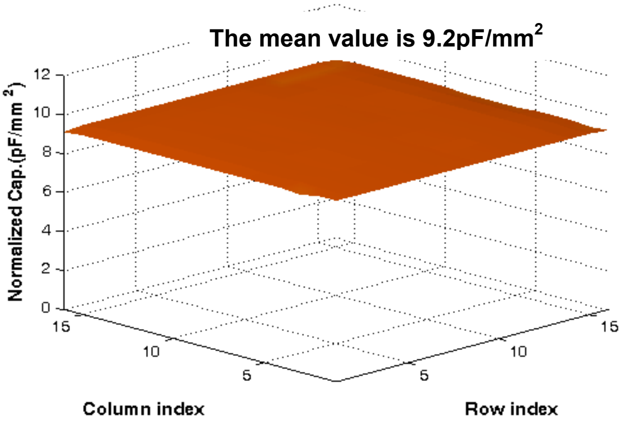


Fig. 52. Typical normalized diode capacitance distribution in a photodiode array for the novel detector micro-module.

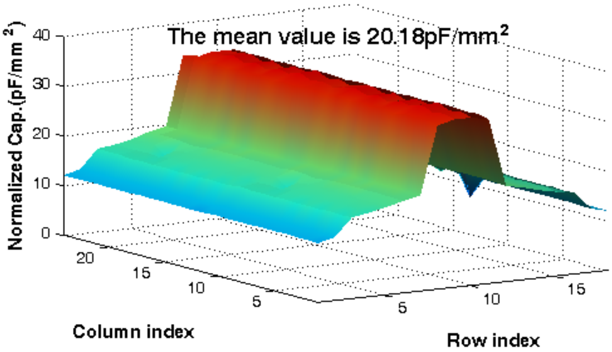


Fig. 53. Typical normalized diode capacitance distribution in a photodiode array for a commercial CT detector module.

4.2 LTCC substrate

LTCC has almost all the merits required for a good CT detector module substrate. With careful control of the process, the LTCC substrate can have excellent surface flatness. A peak-peak distance of 30µm within a 20 x 20mm^2 area is achieved in this study. With the laser-machining process, the machining dimension tolerance can be as low as 5µm. The wiring width and via size can also be very small. Via sizes down to 50µm can be achieved with the present technology of the Microelectronics Laboratory, University of Oulu. An LTCC substrate is mechanically robust, and its CTE is close to that of silicon. Thus, mechanical deformation under temperature variation and other environmental changes is relatively small.

As the chip carrier, the main function of the LTCC substrate in this study is to connect the signal from each individual photodiode cathode node to a specific ball terminal of the BGA. A photograph of the laser cut substrate is shown in Fig.54. Altogether there are 256 bonding pads corresponding to 256 detector pixels. The bottom-view photograph of a LTCC panel that contains 4 substrates is shown in Fig.55. On the bottom there are 325 pads, among which 256 pads are the signal pads and the rest are grounding pads. The substrate consists of 8 tape layers. Each layer is 125µm thick after lamination and firing. The typical trace width used in the design is 200µm. Typical via size is also 200µm.

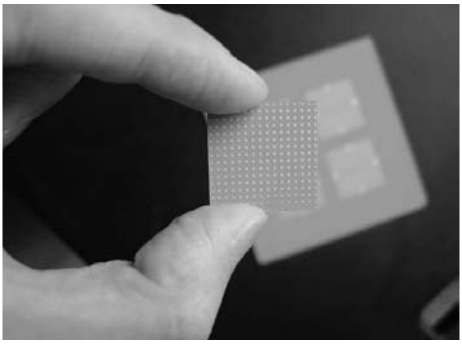


Fig. 54. Top-view of a laser cut LTCC substrate and a panel consisting of four identical substrates before laser cutting.

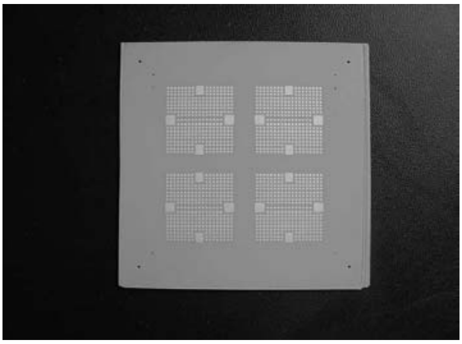


Fig. 55. Bottom-view of a LTCC substrate panel consisting of four identical substrates before laser cutting.

The manufacturing process of the LTCC substrate is shown in Fig.56
The green tape is produced by DuPont. It is first cut into pieces of the same size. Via holes of 200µm diameter are drilled with a laser drilling machine. The via holes are then filled with silver paste by stencil printing with a via-filler. After that, conductive pastes are screen-printed on the via-filled sheet to form conductive traces. On inner layers, silver paste is normally used. On outer layers, silver palladium paste is used to form solderable pads. After trace printing, all the tape layers are aligned and stacked. The stacked multi-layer tapes are then laminated and co-fired.

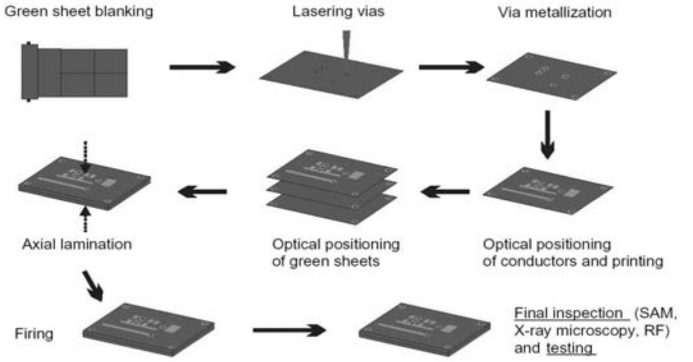


Fig. 56. The manufacturing process of the LTCC substrate in microelectronics lab, Univ. of Oulu .

The paste for the inner conductive layer printing is DuPont Ag6142D. Via-filling paste is DuPont Ag6141. Pads on both the top and bottom layers are printed with DuPont AgPd6138.

After firing, the substrates are cut off from the panel with laser.

Excellent mechanical precision is achieved with our process. The outer dimension error is +/-10µm within the 10 measured samples. The surface profile measurement results show that the maximum flatness error is less than 50µm over a 30.5mm distance. The connectivity of all pads is verified after firing.

4.3 PDA (photodiode array) post-processing

PDA post-processing includes two steps, solderable metal coating and solder mask printing.

4.3.1 Solderable metal plating

Since aluminum cannot be soldered with SnPb based solder, solderable metal layers, mainly nickel, are coated on the aluminum layer on both the top and the bottom of the PDA chip.

When selecting the solderable metal material, the same principles as are used in flip-chip bonding can be applied.

i. The metal needs to have good adhesion to aluminum;
ii. It shall be a good barrier material in preventing diffusion of the solder metals;
iii. It shall also have good adhesion to solder materials. (Tummala 2001)

A SEM (Scanning Electron Microscope) picture of a solder joint on the plated chip is shown in Fig. 57. The nickel layer thickness is about 3 µm. Nickel has diffused into both aluminum layer and solder layer, indicating good adhesion to the chip and to the solder joint.

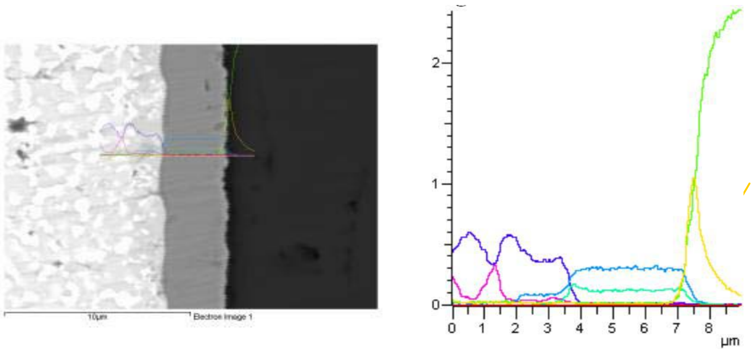


Fig. 57. SEM picture of a solder joint between the PDA and the substrate, the PDA is coated with solderable metal layers.

The PDA is measured after the coating procedure. The results are summarized in Table 4. It can be seen that the plating procedure has little impact on diode characteristics.

Table 4. Comparison of the diode measurement results before and after Ni coating.

@25 °C	Before coating	After coating
Series resistance	5-7 Ω	5-7 Ω
Dark current @10mV	~0.4pA	~0.4pA
Cap. @0V, 100kHz	~12pF	~12pF
Breakdown voltage	> 5V	> 5V

4.3.2 Solder mask coating

After the metal plating process, the bottom of the PDA die has been plated with a solid plate of solderable metal. Before it is soldered to the LTCC substrate with 256 separated joints, in order to prevent solder creeping across the joints and to sustain the height of the solder joints, solder mask is printed on the bottom of the PDA die, leaving openings only over the areas which need to soldered to the substrate pads.
A photograph of the bottom of the PDA die before and after solder mask printing is shown in Fig.58.

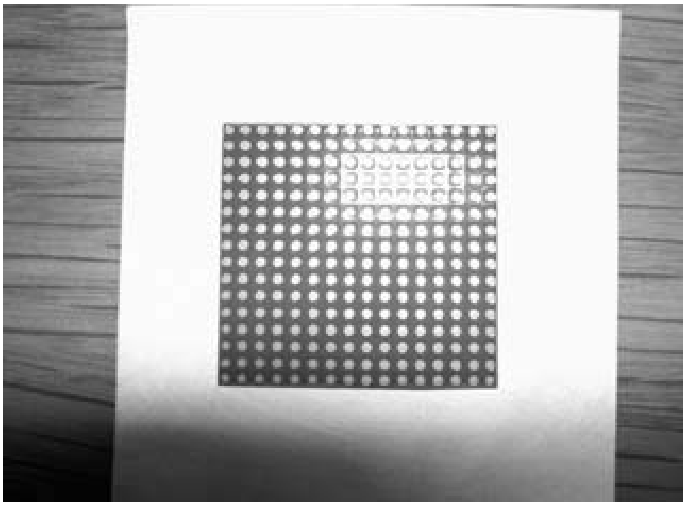
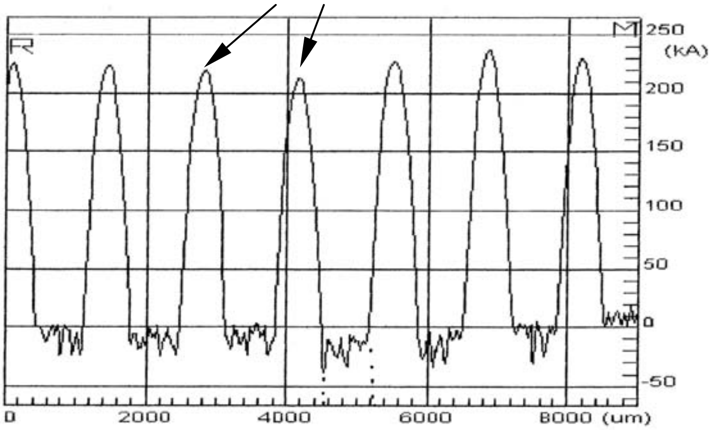


Fig. 58. Bottom view of the PDA die after solder-mask-coating.

The coated solder mask layer thickness is about 23µm. The surface profile of the PDA backside surface with coated solder mask layer was probed with a surface profiler. The result is shown in Fig.59.



Peaks formed by solder mask

Fig. 59. PDA backside surface profile after solder mask coating; As seen, the solder mask layer thickness is about 23µm.

4.4 Other assembly processes

4.4.1 Die-bonding

Solder paste is coated on the pads on the LTCC substrate topside and on the backside of the photodiode array. The solder ball array is applied, then the PDA die is flip-sided and attached to the substrate with a flip-chip bonder. The solder mask openings on the backside of the PDA die are finely aligned with the pads on the top of the substrate. After that the bonded module is re-flowed. A side view microscope picture is shown in Fig.60. The photodiode characteristics are measured before and after re-flow to monitor the influence of the re-flow and the other relevant assembly steps. As shown in Table 5, the results suggested that the diode characteristics are not affected.

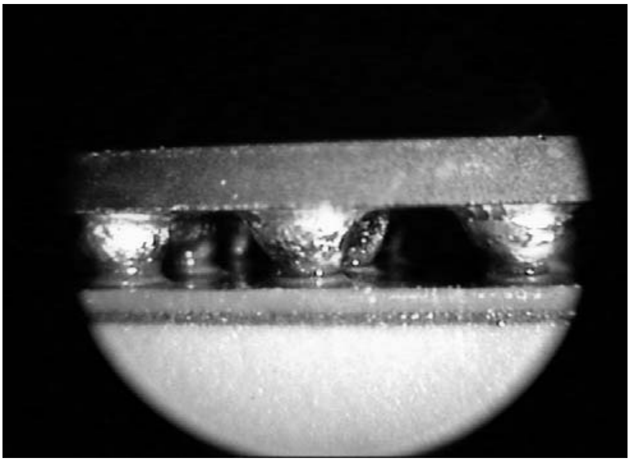


Fig. 60. A microscope picture of a flip-chip bonded photodiode array, the gap between the silicon chip and LTCC substrate is approximately 0.5mm.

Table 5. Comparison of the diode measurement results before and after re-flow.

@25 °C	Before re-flow	After re-flow
Series resistance	5-7 Ω	5-7 Ω
Dark current @10mV	~0.4pA	~0.4pA
Cap. @0V, 100kHz	~12pF	~12pF
Breakdown voltage	> 5V	> 5V

4.4.2 Under-filling and pixel-dicing

Low viscosity dielectric material is fed into the cavity gap between the PDA chip and the substrate. Driven by the capillary force, the under-fill fluid spreads and fills the cavity between the PDA die and the substrate.

The epoxy viscosity and the cavity gap width are the two most important factors in the under-filling process. The process is shown in Fig.61.

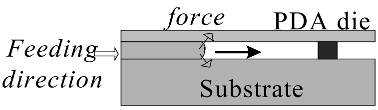


Fig. 61. Under-filling driven by the capillary force.

After under-filling, the photodiode array was diced into separate pixels. The dicing saw should dices through the PDA die, but not down to the surface of the substrate. Maintaining enough solder joint height and good under-filling are the most crucial factors for pixel-dicing.

The under-filling quality is checked with a scanning acoustic microscope (SAM) by scanning the acoustic reflective interface between the PDA chip, the solder balls and the substrate. The SAM pictures of before and after under-filling are shown in Fig.62.

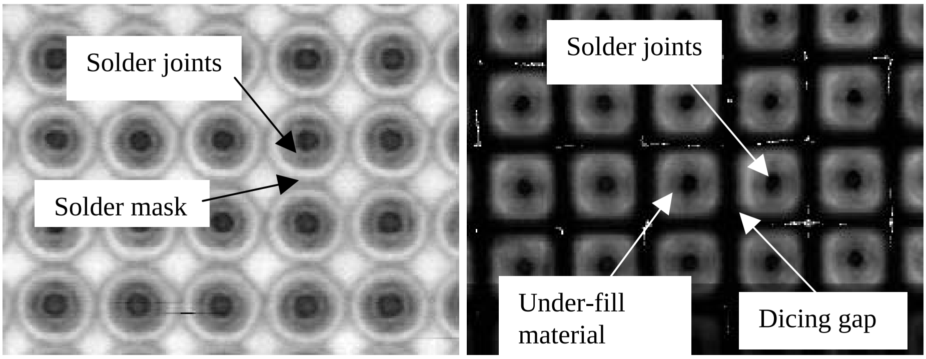


Fig. 62. SAM picture of the PDA, solder balls and under-filling; Left: before under-filling; Right: after under-filling and pixel dicing.

Excellent surface flatness is maintained during pixel-dicing. SEM pictures are taken to check the dicing quality. They are shown in Fig.63.

Diode characteristics measurements are done before and after the pixel-dicing. The results are shown in Table.6. The dark current level is increased 30 – 100%. As analyzed in chapter 3, the influence on the noise performance caused by this change is negligible. Other characteristics are little affected by pixel dicing.

Table 6. Comparison of the diode measurement results before and after pixel dicing.

@25 °C	Before pixel dicing	After pixel dicing
Series resistance	5-7 Ohm	5-9 Ohm
Dark current @10mV	~ 0.4pA	~ 0.6 – 0.9pA
Cap. @0V, 100kHz	~12pF	~12pF
Breakdown voltage	> 5V	> 5 V

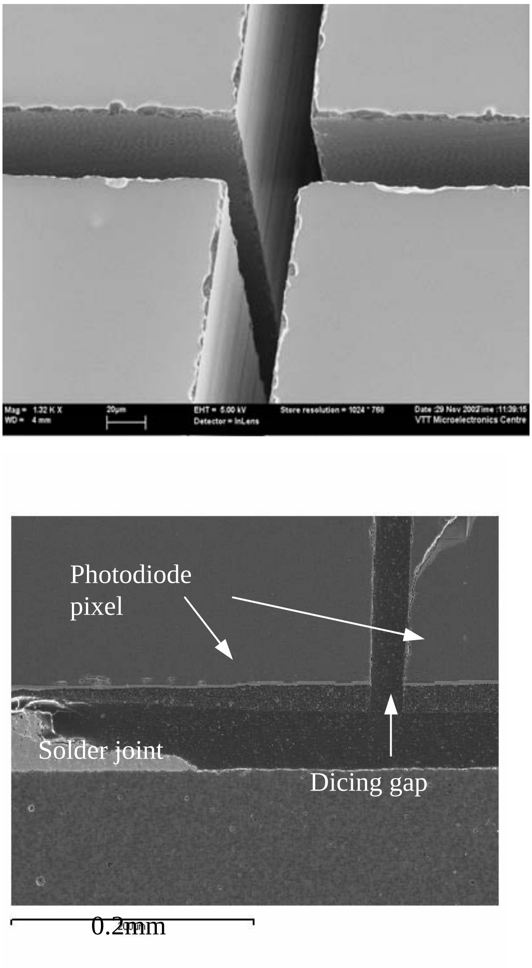


Fig. 63. SEM picture of the micro-module cross-section after pixel dicing; Upper: top view; Lower: Cross-section

4.4.3 Anode connection

In this step, anode contact pads of all 256 pixels on the top-side of the PDA were electrically joined together by soldering to a thin flat metal mesh. This includes four sub-steps; anode mesh growing, lithography on the module, die-attaching and re-flow.

- Anode mesh

The pattern of the metal mesh is shown in the right hand picture in Fig.64. It is a thin layer of metal of the same size as the photodiode array chip. Windows are opened at the active area of each detector element to let scintillation light signals pass. The metal lines

in the mesh block the gaps among the active elements. Pads are made for every active element at the location corresponding to the anode pads on the photodiode array chip. These pads will be soldered to their corresponding pads on the photodiode chip.
The metal meshes were grown on a large flat substrate by an additive method. A large number of meshes can be grown on one substrate at the same time, as shown in the left hand picture in Fig. 64. The metal growing method was developed in the Adjo project at the Microelectronics Laboratory in the University of Oulu.

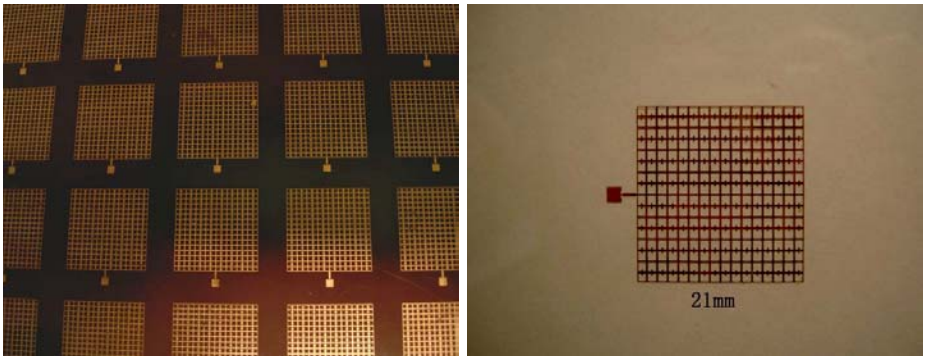


Fig. 64. The metal mesh for top anode connection in the micro-module, Left: pattern of metal mesh grown on the substrate; Right: a close view of one mesh.

- Lithography

In order not to contaminate the photodiode active area during the subsequent assembly, especially the soldering process, a protection layer is needed to cover the active area. A photoresist film is used for this purpose.
A thin photoresist layer is deposited on the top surface of the photodiode array chip after pixel-dicing. A lithography process is performed to make openings on every anode pad. A picture of anode openings after lithography is shown in Fig.65.

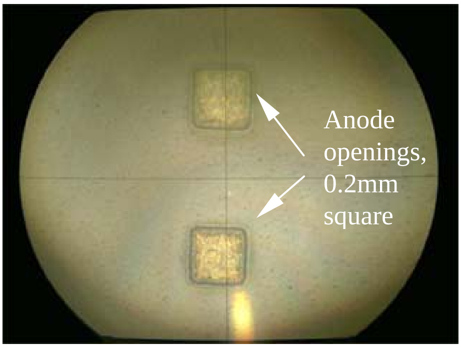


Fig. 65. The top-view microscope picture (10x) of two anode openings after lithography.

Diode characteristics are measured after the lithography process. The results show little difference from the results before the process.

- Mesh attaching and re-flow

After the top anode openings are made, solder paste drops are deposited on the opened anode pads. After that, the micro-modules are flip-sided attached onto the thin metal mesh array, which is still on the flat substrate, as introduced in Fig.64. Then the whole panel with the attached modules is re-flowed. At every detector element, a solder joint is formed between the pad on the metal mesh and the top anode pad on the photodiode. After that, the module can easily be removed from the panel substrate.
The picture of a module with top anodes grounded with the mesh is shown in Fig.66.

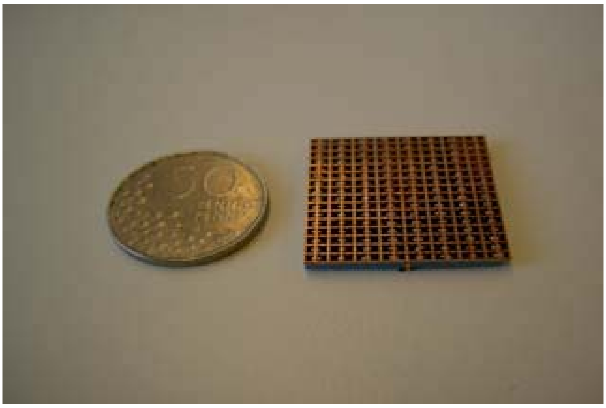


Fig. 66. The micro-module with top anodes grounded with a metal mesh, the size of the micro-module is about 21 x 21mm^2.

The diode characteristic measurement results before and after this process are compared in Table 7. The results show little change.

Table 7. Comparison of the diode measurement results before and after top anode connection.

@25 °C	Before	After
Series resistance	5-9 Ohm	7-8 Ohm
Dark current @10mV	~ 0.6-0.9pA	~ 0.7 – 0.9pA
Cap. @0V, 100kHz	~12pF	~12pF
Breakdown voltage	> 5V	> 5 V

4.4.4 BGA bonding and scintillator attachment

High lead solder spheres are used as the BGA. After BGA bonding and re-flow, there are 325 balls within about a 21 x 21mm^2 area. The pitch distance between two neighbouring terminals is roughly 1.1mm.
A picture of the micro-modules after BGA bonding is shown in Fig.67.

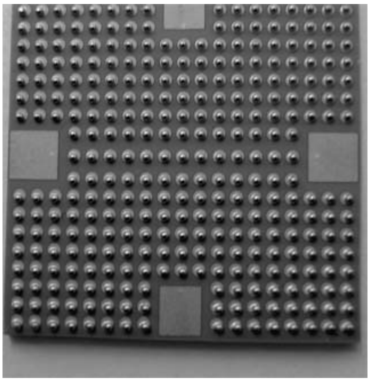


Fig. 67. The BGA on the back-side of the novel micro-module (21 x 21mm^2).

The scintillator can be attached after the BGA bonding and re-flow are completed.

4.5 Tileability

A 64-slice detector module may be realized by tiling 4 detector micro-modules in a row. The picture is shown in Fig.68. To assemble a detector module like this, a module-level PCB with 4 sets of pads is first manufactured. Each set of the pads corresponds to the backside BGA of the detector micro-module. Each signal pad is connected either to a read-out ASIC or to a connector.

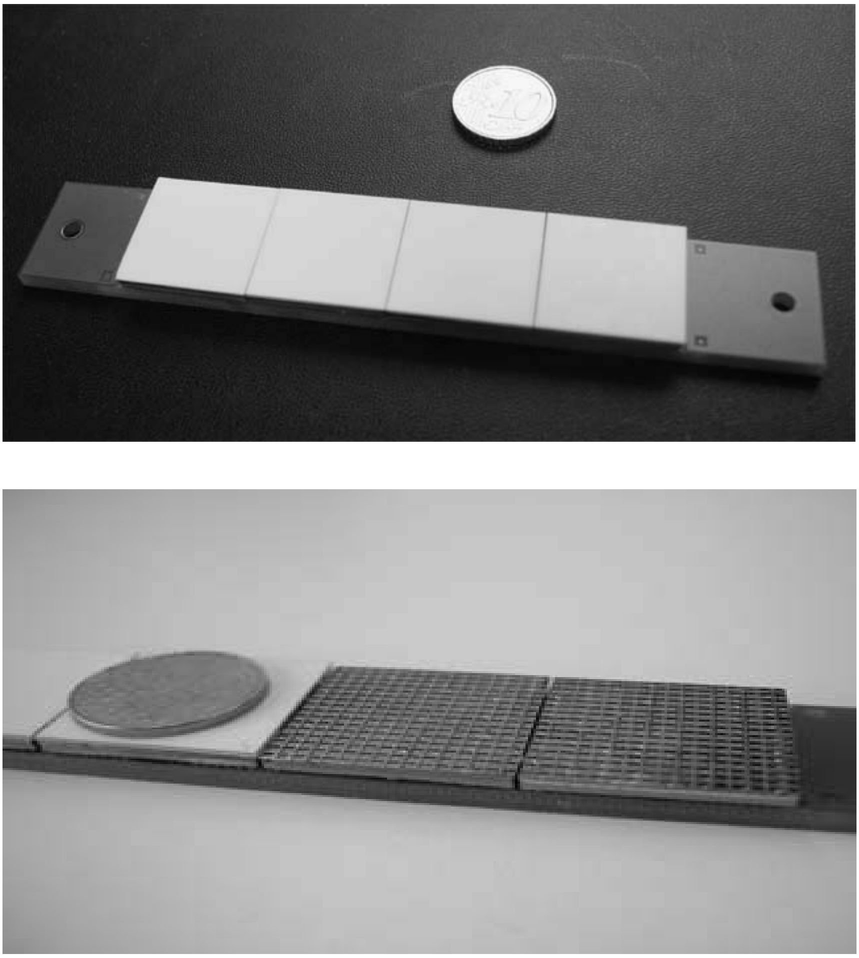


Fig. 68. A 64-slice detector module assembled by tiling four micro-modules.

Solder paste is printed on the PCB pads. The completed detector micro-module is then placed on the PCB and the PCB is re-flowed. After that, the cavity among the BGA balls is filled with the under-fill. The technique is similar to that used in the previous die-bonding under-fill process.

Many detector modules like Fig.68 can be tiled together to form a CT detector arc, as shown in Fig.30 in Chapter 3.

A 64-slice detector module is assembled to show the concept. It is obvious that detector modules with more slices can be assembled in a similar way. Thus a detector array with an unlimited number of detector pixels can be produced.

5 Module measurement results and discussions

In this chapter, the module-level measurement results of the completed novel detector micro-modules are presented and discussed.

In the test, two novel detector micro-modules are assembled side by side on a test board with the method discussed in Chapter 4. The test board assembled with two micro-modules is shown in Fig.69. Each signal node of the micro-modules is connected to one connector pin on the board.

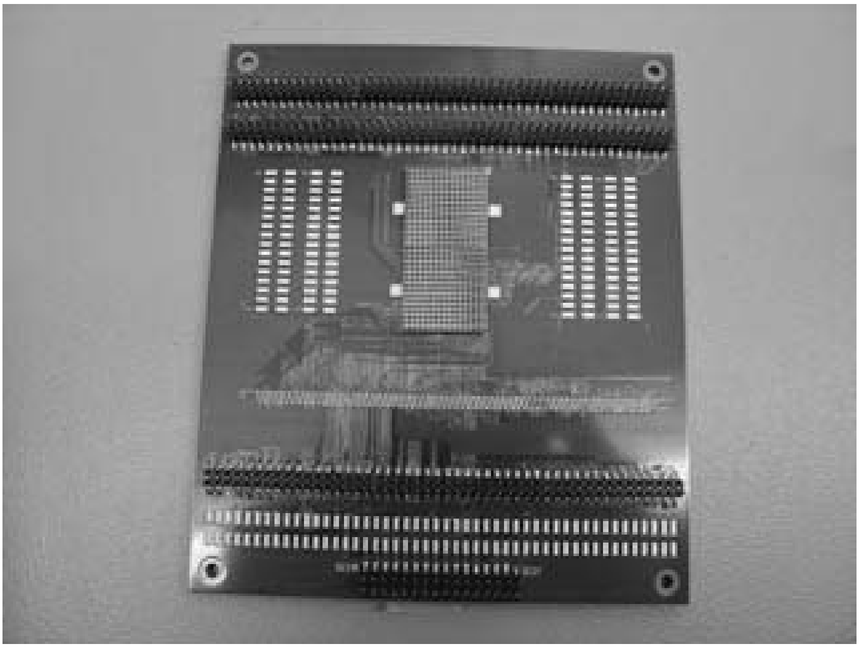


Fig. 69. The picture of the test board assembled with two tiled novel detector micro-modules.

The detector characteristics, i.e. the dark current, the capacitance and the series resistance are measured from the connector on the test board. The light response of the novel micro-modules is also measured with this test board under a parallel light source. Details of the test board and the detector array light test setup are presented in Appendix III.

5.1 Basic detector characteristics measurement results

Typical capacitance distribution over the novel detector micro-module is shown in Fig. 70.

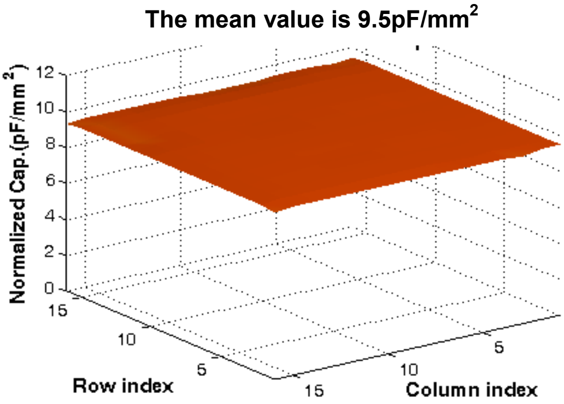


Fig. 70. Capacitance distribution over the novel detector micro-module.

The module-level measurement results are very close to the photodiode array chip-level measurement results, shown Fig.52. This is again due to the short routeing distance, and therefore low parasitic capacitance, in the signal path. The results also show that the capacitance is evenly distributed over the array. As concluded in chapter 3, the noise level is mainly associated with the input capacitance. Therefore, a low detector capacitance reduces the system noise level. Evenly distributed capacitance makes the noise also evenly distributed. Both are crucial to achieving good image quality.

The detector dark current of the novel micro-module is shown in Fig.71.

At 10mV bias voltage, the dark current typical value is around 0.7 – 0.9pA. Compared with the PDA dark current results shown in Fig.46, the dark current is approximately doubled. This is mainly caused by the mechanical stress introduced by the pixel dicing. However, as previously concluded, the dark current shot noise makes a negligible contribution to the system noise performance. With equation (3.2), the noise contributed by the dark current can be estimated. In application, since the detectors are zero biased, the dark current shall be much lower than at 10mV bias, consequently the shot noise PSD is 3.2E-31A^2/Hz, which is negligible compared to other noise source.

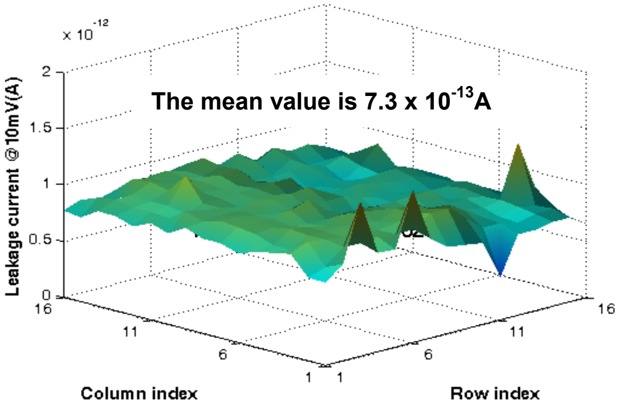


Fig. 71. Typical results of the dark current measured from the completed novel micro module.

The series resistance of the novel micro-module is shown in Fig.72. When compared with the series resistance measured from the photodiode array chip, it is clearly seen that the assembly process does not cause extra parasitic resistance. The apparent difference in the mean value for the two cases is due to the precision of the measurement device.

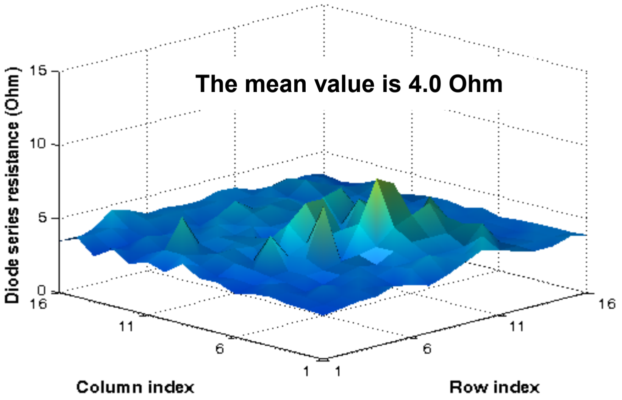


Fig. 72. Typical series resistance of the novel detector micro-module.

5.2 Light response measurement results

In the test, the output photocurrents of each element of the novel micro-modules are measured. As a comparison, a conventional CT detector module product is also measured under the same light illumination. For the convenience of comparison, the light response measurement results of both modules are normalized to the active area of the corresponding detector elements. A typical result for a novel micro-module is shown in Fig. 73 together with a typical result for the conventional CT detector module product.

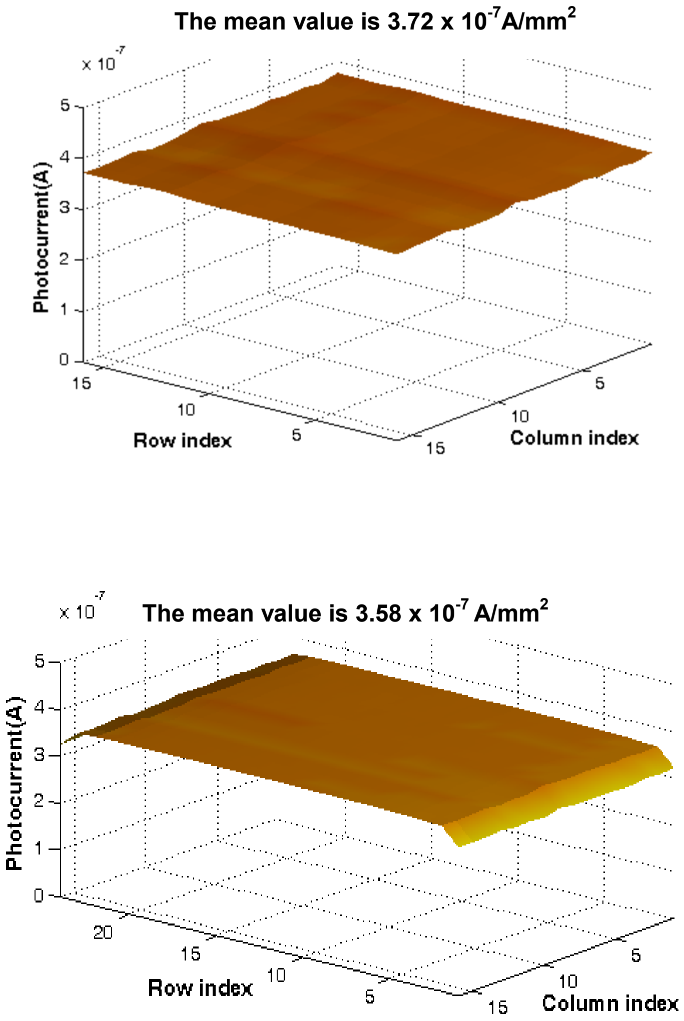


Fig. 73. Typical photocurrent density of the novel detector micro-module and a conventional CT detector module product measured at the same light intensity; Upper: the results of the novel detector micro-module; Lower: the results of the conventional CT detector module.

As it is shown in Fig.73, the photocurrent density of the novel detector micro-module is very uniform over the array. The mean value of the photocurrent density of the novel micro-module is only slightly higher than that of the conventional CT detector modules. Because a white light source is used in the light response measurement, the measured photocurrent is an integral over the whole light spectrum. If a light source with an emission wavelength within the wavelength of interest, i.e. the emission wavelength of the common scintillator materials, had been used, the difference would have been higher.

Fig.73 proves that the novel micro-module has a good light response and a high uniformity among the channels. Therefore it is suitable for scintillation-based X-ray detection applications.

During the thesis work, the novel module could not be tested with X-rays due to the very high tooling cost of customized scintillator manufacturing and the limited time scale. The test will be conducted when the external financial source is located. However, the purpose of the thesis is to verify the concept and the feasibility of the novel detector micro-module. Because the scintillator for the novel micro-module is in principle the same as that for the conventional CT detector modules, there is no difficulty or novelty in producing the scintillator. Therefore, the feasibility of the novel detector micro-module has been verified after the light response is verified.

5.3 Future development

The novel detector micro-module can be improved in several respects.

In this thesis, the effects of dicing on the photodiode dark current are only studied preliminarily. It is concluded that dicing may raise the photodiode dark current level and raise the deviation of the dark currents. More studies shall be carried out to find the optimized compromise between the photodiode performance and the dicing margin of photodiode chips. The minimum pixel size for the novel detector micro-module shall be found out. More studies shall also be carried out to give better control to the dark current performance of the novel micro-module in industrial scale production. In order to achieve as large active area as possible, measures to minimize the dicing margin shall also be investigated.

One possible improvement to make is to have an additional N implantation outside the active area to make higher the N-doping around the active area. Due to the higher N doping, the extension of the PN depletion region on Si-SiO_2 interface would be smaller. In other words, the surface depletion region is more constrained towards the active area, and therefore is farther away from the dicing edge. Consequently, mechanical damages caused by dicing would have less effect on the depletion region.

Now the metal mesh for top anode connection is made of copper. Because copper is prone to erosion, coating the copper mesh with noble metals, for example, a thin layer of gold, shall be investigated.

For CT systems with more than 64 slices, the routing of the module-level PCB (the board which carries the novel detector modules, as shown in Fig. 68) is difficult due to the large amount of signal lines. For example, for a 128-slice module, the number of inputs and outputs is 4096. The number of I/O pins can be reduced by assembling a read-out ASIC to the backside of the novel micro-module. Ideally, the ASIC would include parallel current signal readout, current-voltage conversion and A/D conversion. When this is realized, the output pin numbers of the detector module PCB could be reduced by 95%. The system integration of the novel micro-module will become easier. To realize the integration of the read-out ASIC to the backside of the micro-module, a cavity on the backside of the LTCC module may be needed to contain the ASIC.

6 Conclusions

To make detector modules with an unlimited number of slices is a day dream in CT technology. It has been the target of this thesis to meet this demand. The novel concept of a “detector micro-module” has been proposed, investigated, realized and characterized.

In the novel detector micro-module, photocurrent signals are read out from the bottom side of the photodiode array chip via the silicon bulk. By avoiding the use of the top surface of the chip for routeing, as is the case in conventional CT modules, rectangular detector building blocks containing a certain number of detector elements can be produced. By tiling such building blocks in both x- and y-directions in a plane, detector arrays with any number of detector elements (in multiples of the number in a single building block) can be built. This cannot be achievable by the conventional method.

The novel detector micro-module presented in this thesis contains 16x16 active pixels and the size of the array is about 21 x 21mm^2. The array of detector pixels is soldered to a multilayer LTCC (low temperature co-fired ceramics) substrate via a BGA (ball grid array) with each pixel soldered onto one solder sphere. Photocurrent signals are read out from the “cathode node” (N node) of the photodiode via the BGA.

In the conceptual verification phase, the effect of dicing on the dark current of a small pixel detector was firstly been verified and found to be acceptable for CT applications. By utilizing thermo-mechanical modeling and simulation of the micro-module structure it was concluded that the mean stress a micro-module experiences during the high temperature assembly process is lower than that in the conventional CT detector modules. A thorough analysis of the characteristics of the pre-amplification electronics was conducted. It was concluded that the detector capacitance has a dominating effect on system noise. Therefore, it was concluded that the novel detector micro-module is superior to the conventional modules due to its low parasitic resistance and capacitance.

The PDA design, manufacturing process and measurement results were discussed. Compared to a conventional PDA product for CT applications, the light sensitivity does not exhibit interference peaks and valleys and is therefore smoother. It is also about 10 – 20% higher in the wavelength range of interest. With the improved processing procedure, the photodiode dark current was found to be extremely low. The typical value was about 30pA/cm^2, the lowest reported so far.

A multi-layer LTCC substrate with 8 tape layers was designed and manufactured to be the substrate of the novel micro-module. The conductive line feature width was 150um and the via hole feature diameter was 200um. Excellent mechanical precision was achieved, which is crucial for realizing the assembly and tileablity of the novel CT detector micro-modules. The outer dimension accuracy was found to be within +/-10um. The surface flatness is less than 50um over 30.5mm distance.

An assembly process flow was designed and developed to assemble and manufacture the novel micro-module. After each individual assembly step, the PDA was measured to monitor and analyze the effect on the detector performance caused by the assembly step. It was found that the whole assembly process flow has only a negligible effect on the detector performance. The detector light-sensitive surface is maintained with good flatness. The completed micro-module showed good dark current performance and extremely low wiring parasitic capacitance and wiring parasitic resistance. The light response of the completed micro-module was also verified and good response uniformity observed. A 64-slice detector module was made successfully by tiling the novel micro-modules. In this thesis, the exemplary detector pixel pitch size was approximately 1.4 x 1.4mm^2. However, with the same methodology, a smaller pixel pitch can also be achieved as well.

Compared with the present commercial CT detector modules, the novel micro-module has been shown to be advantageous in the following respects; (i.) The micro-module can be tiled to produce detector modules with an unlimited number of slices, while 64-slices is the maximum achievable with conventional approaches; (ii.) The novel micro-module has a smoother light sensitivity curve, and will therefore exhibit a better response uniformity in the system level in volume production; (iii.) The novel micro-module has nearly zero parasitic capacitance compared to up to 20pF in commercial CT detector modules. It also has nearly zero parasitic resistance compared to tens of ohms or more than one hundred ohms in many of the present CT detector module products.

Compared with the other contemporary solutions, the novel micro-module is also advantageous in many other respects. The novel micro-module does not require any significant change to the silicon wafer processing. This is important because such changes may degrade detector performance. The manufacturing cost is also relatively low.

In short, this thesis concluded that the novel detector micro-module has successfully produced, its performance has been verified and meets the demand of the CT industry and the advancing CT technology.

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Appendices

Appendix 1: Photodiode Spectral Sensitivity Measurement Setup

The photodiode spectral sensitivity is measured by the system shown in Fig.A1.1.

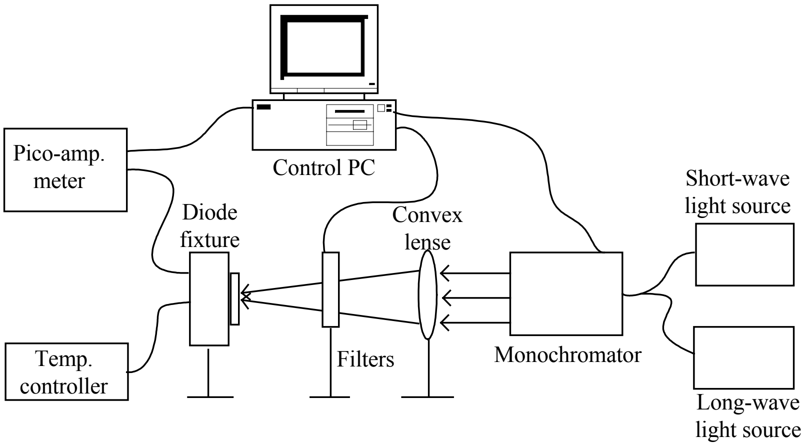

Fig.A1.1. Photodiode spectral sensitivity measurement setup.

Two light sources are employed to cover the spectrum from 200 to 1040nm. Light is feed into the monochromator via optical cables. The monochromator is a band-pass light filter. It outputs the light at the wavelength specified by the control PC via its serial port and suppresses the light at other wavelengths. The output parallel light beam is focused with a convex lens to form a light spot as small as 0.5mm. The light filter set is used to further screen out the stray light or the 2nd order light generated by the monochromator. The filter in the filter set can also be selected by the control PC. The diode fixture holds the photodiode under test mechanically. It also provides the signal pin connection which is connected to a pico-amp meter via a coaxial cable. The diode fixture also contains a Peltier device to control the temperature of the diode which is set by a separate temperature controller. The pico-amp meter can measure current signals down to sub-pico amperes. The measured data is sent to the control PC via a GPIB interface.

The measurement procedure is coordinated by the control PC.

To avoid external EMC noise and light noise, the whole system is shielded in a grounded dark box.

Measurement precision down to the sub-pico ampere level has been achieved with this system.

Appendix 2: Material properties used in the thermal-mechanical modeling and simulation of the novel detector micro-module

A few important assumptions are made in the simulation.

- All materials are linear and isotropic (except FR4 which is orthotropic),
- There are only elastic stresses (no phenomena such as creeping, plasticity, etc.),
- Ambient temperature Ta = 25° C,
- All epoxies behave as linear elastic materials, i.e. the operating temperature is below the Tg (glass transition temperature),
- There are no transition areas between materials,
- The applied temperature is uniform within the module (there are no temperature gradients),
- The module is in thermal steady-state,
- The material properties are constant over temperature.

Table A2.1. The material properties used in the simulation.

Material	CTE [ppm/K]	Modulus of elasticity [GPa]	Poisson's ratio [-]	Tensile strength [MPa]	Specific heat [Ws/kgK]	Thermal cond. [W/mK]	Density [kg/m^3]
LTCC (DuPont)	7.0	75.0	0.20	152	740	3.0	3100
Silicon	2.8 129	0.28	81	712	120.0	2330	
Au	12.0	80.0	0.30	130	130	130.0 (film)	18900
Glob top	60.0 180.0	10.0	0.33	69	1700	1.5	1800
Sn10Pb90 solder	28	19.0	0.35	30	178	37.0	11000
Optical epoxy	45.0 157.0	1.70	0.33	69	2400	1.0	1200
PCB FR4	18.0 (x,y) 50.0 (z)	20 (x,y) 10 (z)	0.38	250	1000	0.8 0.3	1800
Conduct. epoxy	38.0 125.0	1.86	0.33	69	2400	0.5	1200

Appendix 3: Detector Array Light Response Test System

I. Light sensitivity uniformity test

The light sensitivity uniformity test system is shown in Fig.A3.1.

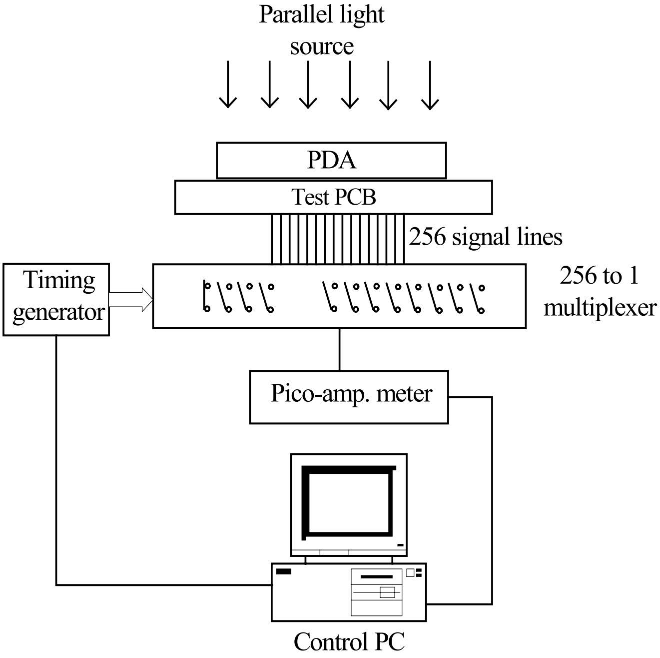

Fig.A3.1. The diagram of the light sensitivity uniformity test system

The PDA to be tested is fixed under a parallel light illumination source. Each pixel of the PDA is routed to one channel of the 256 to 1 multiplexer. The multiplexer is controlled by a programmable logic device, which interpret the commands from the control PC and sends corresponding control logic signals to the multiplexer. The multiplexer output is connected to the pico-ampere meter. The pico-ampere meter measures the current signal and sends the results to the control PC via the GPIB interface.

In a normal measurement, the control PC sends commands to read from channel No.1 to channel No.256.

The test PCB is shown in Fig. A3.2.

Two micro-modules can be assembled side by side on the board. The concept of tileablity is verified in this way because any number of micro-modules can be tiled in the same way. Signals are read out from the pin array surrounding the two micro-modules.

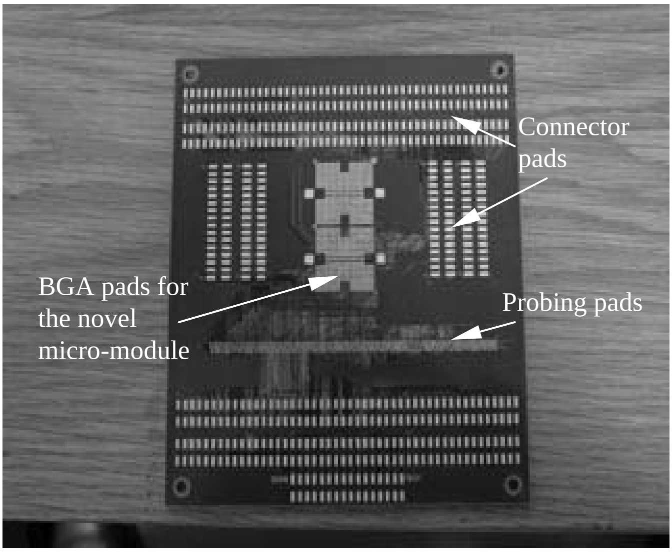

Fig.A3.2. The PCB for the testing of the novel detector micro-module

Appendix 4: Photodiode Dark Current Measurement System

The photodiode spectral sensitivity is measured in the system shown in Fig. A4.1.

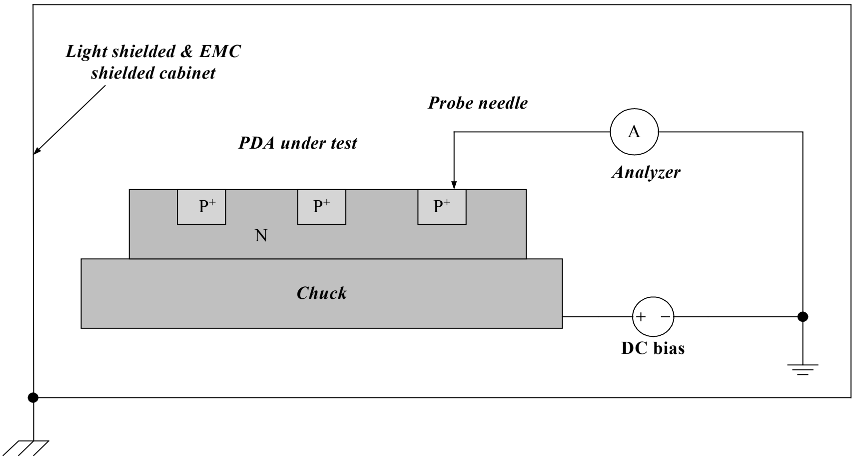

Fig.A4.1. Photodiode dark current measurement system

The whole system is contained in a cabinet which is both light-shielded and EMC-shielded.

The photodiode array under test is fixed on a metal chuck by vacuum. The backside metallization of the photodiode array touches the metal chuck, therefore an electrical contact is made. In a measurement, a probe needle touches the anode pad of one detector pixel. A HP4145 is employed to provide the required DC reverse bias to the photodiode array and also measure the electrical characteristics of the array.

With this measurement system, the photodiode dark current, the dynamic resistance and the breakdown voltage can be measured.

In an automatic array measurement, the chuck moves to connect every pixel one by one to the probe needle according to the pre-defined array map.

The measurement system is able to measure leakage currents down to tens of fA.

Appendix 5: Photodiode sensitivity measurement results

The spectral sensitivity curve of the photodiode for the novel detector micro-module is shown in Chapter 4, Fig.47. The numerical values of the curves shown in Fig.47 are shown in the following table, Table V.1. The measurement results in the following table are measured from PCM photodiode in size of 2.5x2.5mm^2. The "100% quantum efficiency" is the sensitivity assuming 100% quantum efficiency.

Table A5.1. Numerical values of the sensitivity curves shown in Chapter 4, Fig.4.7.

Wavelength (nm)	The novel micro-module (A/W)	100% quantum efficiency (A/W)	A conventional module (A/W)
400	0.110	0.322	0.057
420	0.163	0.338	0.066
440	0.208	0.354	0.073
460	0.249	0.370	0.096
480	0.283	0.386	0.148
500	0.310	0.403	0.242
520	0.334	0.419	0.286
540	0.364	0.435	0.294
560	0.377	0.451	0.286
580	0.390	0.467	0.281
600	0.408	0.483	0.290
620	0.422	0.499	0.314
640	0.438	0.515	0.352
660	0.449	0.531	0.404
680	0.469	0.547	0.445
700	0.459	0.564	0.489
720	0.468	0.580	0.522
740	0.484	0.596	0.530
760	0.493	0.612	0.520
780	0.503	0.628	0.509
800	0.505	0.644	0.485
820	0.497	0.660	0.479
840	0.483	0.676	0.454
860	0.466	0.692	0.430
880	0.434	0.708	0.404
900	0.387	0.725	0.375
920	0.347	0.741	0.338
940	0.295	0.757	0.299
960	0.233	0.773	0.249
980	0.182	0.789	0.197
1000	0.135	0.805	0.154