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Guoyong Duan

THREE-DIMENSIONAL EFFECTS AND SURFACE BREAKDOWN ADDRESSING EFFICIENCY AND RELIABILITY PROBLEMS IN AVALANCHE BIPOLAR JUNCTION TRANSISTORS

UNIVERSITY OF OULU GRADUATE SCHOOL;
UNIVERSITY OF OULU, FACULTY OF TECHNOLOGY,
DEPARTMENT OF ELECTRICAL ENGINEERING;
INFOTECH OULU

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Academic dissertation to be presented with the assent of the Doctoral Training Committee of Technology and Natural Sciences of the University of Oulu for public defence in OP-sali (Auditorium L10), Linnanmaa, on 1 March 2013, at 12 noon

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Abstract

Although avalanche switching has been known since the 1950s, a trustworthy one-dimensional physical interpretation of the practically interesting high-current mode ("secondary breakdown") in a Si avalanche transistor has appeared only within the last decade and thanks to numerical one-dimensional and two-dimensional physics-based device modelling. A good fit with experimental waveforms has been achieved only for high-current, long-duration pulses (~100 A/7 ns), however, and modelling fails in the case of shorter pulses in a range that is of greater practical importance. One significant finding in this thesis is that reliable modelling of a Si avalanche transistor is in general impossible without taking account of three-dimensional effects. The task is a challenging one, as it is being put forward for the first time and state-of-the-art simulators are unable to model three-dimensional avalanche dynamics with an external circuit included (i.e. in “MixedMode”). Thus a smart approach was adopted which allowed the main features of the three-dimensional transient to be explained using a two-dimensional simulator and compared with the experimental data. The focus was on a trade-off of between high switching efficiency in an avalanche transistor (high-speed switching with a lower residual voltage as occurs at extremely high current densities) and device reliability as determined by local overheating during a single pulse, similarly resulting from high current density. This denotes the practical importance of the work performed here, as the current density is directly affected by three-dimensional dynamic processes.

The second task performed in this thesis concerns the reliability of the GaAs avalanche transistors developed recently in the Electronics Laboratory and demonstrated of unique (superfast) switching and high-power-density sub-THz emission for mm-wave imaging and radars. Critically important for this new device is the limitation originating from premature breakdown at the surface of the GaAs p-n junction with a high density of surface states. Two of the results of this work are also fairly challenging: (i) the mechanism of "soft" surface breakdown intrinsic to all GaAs transistor mesas was interpreted in terms of the surface trapping of avalanche-generated electrons as suggested here, and (ii) passivation of the surface with a chalcogenide glass was suggested, as this allows the premature surface breakdown to be suppressed completely, an effect that has proved to be caused by a large negative surface charge formed on the “U centres” intrinsic to a chalcogenide glass.

Keywords: avalanche breakdown, bipolar junction transistors, experiment, high speed switch, simulation, surface breakdown

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Tiivistelmä

Vaikka avalanche läpilyönti pii-transistoreissa on tunnettu jo 1950-luvulta lähtien, luotettava 1-dimensionaalinen fysikaalinen tulkinta ilmiöstä käytännön sovellusten kannalta kiinnostavilla suurilla virtatasoilla (ns. “secondary breakdown”) on esitetty vasta viime vuosikymmenen aikana 1- ja 2-dimensionaalisiin numeerisiin simulointeihin ja fysikaaliseen mallinnukseen perustuen. Kokeellisten mittausten ja simulointien välille on saatu hyvä sovitus kuitenkin vain sellaisessa ohjaustilanteessa, jossa transistori toimii suurella virtatasolla ja tuottaa leveitä virtapulsseja (~100 A / 7 ns); mallinnus ei vastaa mittaustuloksia lyhyillä virtapulsseilla, jotka kuitenkin ovat tärkeitä käytännön sovellusten kannalta. Yksi tämän työn keskeisiä havaintoja on se, että piipohjaisen avalanche transistorin luotettava mallintaminen ei ole käytännössä yleisesti mahdollista ottamatta huomioon 3-dimensionaalisia (3D) efektejä. Tällainen mallinnus, jota tässä työssä on kehitetty ensimmäistä kertaa, on vaikeaa, koska kaupalliset simulointiohjelmistot eivät kykene käsittelemään avalanche ilmiön dynamiikka 3-dimensionaalisesti tilanteessa, jossa transistoriin on kytketty ulkoinen piiri (ns. mixed-mode -simulointitilanne). Tähän kehitettiin tekniikka, joka mahdollistaa 3-dimensionaalisen kytkentätransientin tärkeimpien piirteiden selittämisen ja mittaustuloksiin vertaamisen 2-dimensionaalisten simulointien perusteella. Erityisesti pyrittiin selvittämään avalanche transistorin korkean kytkentähyötysuhteen (kollektori-emitterin ns. residual-jännitteen käyttäytyminen virrantiheystason mukaan) ja komponentin luotettavuuden välistä riippuvuutta. Luotettavuuteen vaikuttaa olennaisesti komponentin sisäinen, lokalisoitunut lämpötilamaksimi, joka myös riippuu keskeisesti komponentin virrantiheystasosta kytkentäpulssin aikana. Toisaalta virrantiheyteen vaikuttavat juuri komponentin 3-dimensionaaliset dynaamiset prosessit, joten työn käytännöllinen merkitys on suuri.

Työn toisen osa käsittelee elektroniikan laboratoriossa äskettäin kehitetyn GaAs-avalanche transistorin luotettavuutta. Tällaisella transistorilla on demonstroitu olevan erityislaatuinen supernopea kytkeytymisefekti, ja se emittoi korkealla tehotasolla sähkömagneettista säteilyä n. 0,1–1 THz taajuusalueella. GaAs-avalanche transistoria voidaan täten potentiaalisesti hyödyntää mm-alueen kuvantamisessa ja tutkissa. Tämän uuden transistorin luotettavuuteen vaikuttaa ratkaisevasti rajoitus, joka aiheutuu ennenaikaisen, GaAs-pn-liitoksen pinnassa vaikuttavasta suuresta pintatilatiheydestä johtuvan läpilyönnin mahdollisuudesta. Työn kaksi keskeistä tulosta ovat: (i) kaikilla GaAs-transistoreilla ilmenevä ns. ”pehmeä”-läpilyönti aiheutuu avalanche ilmiön synnyttämien elektronien loukkuuntumisesta pinta-tiloihin, ja (ii) pinnan passivointi kalkopyriittilasilla estää läpilyönnin kokonaan, koska kalkopyriittilasille luonteenomaiset ”U-tilat” aiheuttavat liitoksen pintaan korkean negatiivisen pintavarauksen.

Asiasanat: avalanche läpilyönti, bipolaaritransistori, kokeellinen, nopea kytkin, pintaläpilyönti, simulaatio

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Oulu Guoyong Duan

Abbreviations

A	Ampere
ABJT	Avalanche bipolar junction transistors
APD	Avalanche photodiode
BJT	Bipolar junction transistors
C	Coulombs
CCD	Charge-coupled device
e	Electron
E	Electric field
e-b	Emitter-base
EBI	Emitter-base interface
FET	Field effect transistors
h	Hole
HBT	Heterojunction bipolar transistors
j_c	Critical current density
kA	Kilo-ampere
kV	Kilo-volts
L	Light intensity
LD	Laser diode
LED	Light emitting diode
MA	Mega-ampere
MCP	Micro-channel plate
MOSFET	Metal–oxide semiconductor field-effect transistor
N_A	Acceptor concentration (cm^{-3})
N_D	Donor concentration (cm^{-3})
NDM	Negative differential mobility
nF	Nanofarad
ns	Nanosecond
P_{eff}	Effective e-b perimeter
pF	Picofarad
q	Electron charge 1.6×10^{-19} C
THz	Terahertz
T_L	Lattice temperature
υ_n	Electron velocity
υ_p	Hole velocity
v_s	Saturated electron velocity, ~10^7 cm/s for Si and GaAs

List of original publications

This thesis is based on the following original papers, which are referred to in the text by their Roman numerals [I-VII]:

I Duan G, Vainshtein S & Kostamovaara J (2008) Lateral current confinement determines silicon avalanche transistor operation in short-pulsing mode. IEEE Transactions on Electron Devices 55(5): 1229–1236.

II Duan G, Vainshtein S & Kostamovaara J (2010) Self-organizing of avalanche transistor operating area in accordance with parameters of external circuit. Annual Journal of Electronics 4: 26–29.

III Duan G, Vainshtein S & Kostamovaara J (2011) Si avalanche transistor optimized for subnanosecond operation: physics based transient modeling. Annual Journal of Electronics 5: 121–123.

IV Duan G, Vainshtein S & Kostamovaara J (2011) Peculiarities of Surface Breakdown in GaAs Bipolar Junction Structures. IEEE Transactions on Electron Devices 58(8): 2551–2558.

V Vainshtein S, Javadyan V, Duan G, Tsendin K, Hovhannisyan R & Kostamovaara J (2012) Chalcogenide glass surface passivation of a GaAs bipolar transistor for unique avalanche terahertz emitters and picosecond switches. Applied Physics Letters 100(7): 073505 (1–4).

VI Duan G, Vainshtein S & Kostamovaara J (2012) Turn-on spread determines the size of the switching region in an avalanche transistor. Applied Physics Letters 100(19): 193505 (1–4).

VII Duan G, Vainshtein S & Kostamovaara J (2012) Three-dimensional peculiarities in an avalanche transistor provide a broadened range of amplitudes and durations of the generated pulses. Applied Physics Letters 101(17): 173506 (1–4).

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1 Introduction

1.1 Background

The invention in 1947 of the first bipolar transistor started what has been termed a second industrial revolution [1]. After more than 60 years of development, a very large number of semiconductor devices have emerged with Si technology predominating, but with a growing demand for devices based on other semiconductor materials (GaAs, AlAs, GaP, InP, GaN, AlN, SiC, and various solid III-V solutions such as AlGaAs, InGaAsP etc.). The leader in various integrated circuit applications is certainly Si-based MOSFET, and even bipolar junction transistors (BJT) are not so commonly used, while BJT in avalanche switching mode still looks fairly exotic today and many engineers and researchers are not even familiar with its high-current/high-speed modifications. This is not fair, of course, as there are many applications, in which avalanche bipolar junction transistors (ABJTs, see typical structure in Fig. 1) cannot be replaced with any other semiconductor device due to certain very significant advantages, mostly related to nanosecond/sub-nanosecond and even picosecond switching of high currents (~1 A-100 A) for laser diode (LD)-based imaging and radars [2, 3], LED in time-resolved fluorescent studies [4, 5] and generators for optical or electron shutters [6, 7]. Although several commercial types of ABJT are available and are widely used in the generation of high current pulses of a few ns, it seems that they fail to utilise all the advantages offered by avalanche switching. Not all physical aspects of the switching that are of practical importance have been understood completely until now, and even the most critical properties of high-current switching were formulated only within the last decade. This statement sounds strange indeed, as avalanche switching in BJTs has been known since the 1950s, interpretations of this switching are given in dozens of books on semiconductor devices and fairly detailed analytical investigations have been performed [8]. That is true as far as moderate currents (<1 A) and relatively long switching times (~100 ns) are concerned, but much more important and widely used in applications is fast switching (< 10 ns) at very high currents (approaching ~80 A) and extremely high current densities (up to ~ (1–10) MA/cm^2).

Let's make very brief overview of typical application requirements, parameters and properties of the drivers competing with avalanche transistors. One of the most popular applications is pumping of high-power laser diodes in

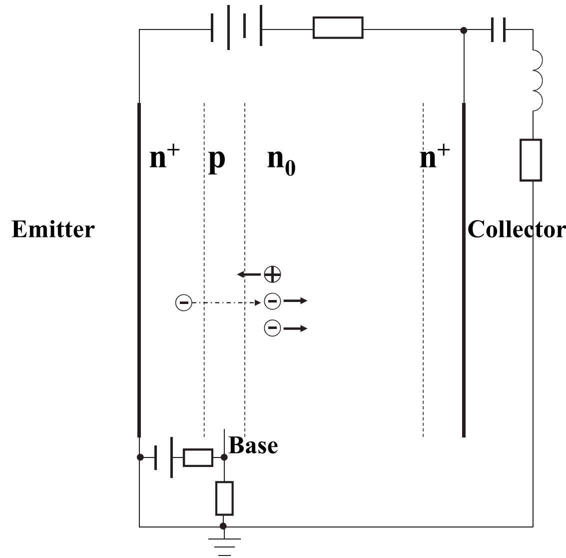

Fig. 1. Illustration of carrier multiplication in the high electric field of the n_0 region of a n^+-p-n_0-n^+ bipolar junction transistor.

the nanosecond range. As soon as it concerns the pulse durations of ~10 ns or longer, most popular and simple is making use of Si FETs. More and more applications, however, require pulse durations of 1–6 ns with the current amplitudes ranging from 3 to 100 A respectively. Moreover, when high-power picosecond-range optical pulses have to be obtained from laser diodes operating in gain-switching or Q-switching mode, the pulse duration is required to be further reduced down to 600–200 ps (the values comparable with lasing delay when the pumping current amplitude exceeds the threshold value by a factor of 3 to 10 respectively). No commercial components are able to satisfy those parameters if the current amplitude has to exceed significantly the level of ~0.1 A. The exceptions are two types of commercial generators: one (http://www.kentech.co.uk) is based (to our information) on a long chain of commercial (nanosecond) avalanche transistors and this chain provides high-voltage (kV range) sub-nanosecond switching. From analyse of literature we think that the physical understanding of this operation mode is lacking, the generators are not very reliable and durable, not compact or cheap. The second type is based on a combination of drift-step-recovery-diodes (DSRD) and silicon avalanche shapers (SAS) [9–13], which is used in a broad class of reliable high-

speed, high-voltage generators (http://www.fidtechnology.com). However they are expensive and not compact as well. All in all, commercial switches, which are able to compete with fast avalanche transistors are lacking.

An additional brief note concerns typical current densities and carrier transport in the switching devices as compared with the avalanche transistors. Traditional high-power switches based on transistors and thyristors operate in quasi CW mode or with pulses in the millisecond range, and the current density there do not typically exceed 100 A/cm^2. The carrier transport is a combination of the diffusion and drift in a moderate electric field. The transistor switches (FETs or BJTs) operating in micro-and sub-microsecond range typically utilize the current density in the range 300–10000 A/cm^2, but never higher. In those switches the carrier transport is mostly determined by the carrier drift within the carrier velocity range between ~10^5 cm/s and ~10^7 cm/s (saturated value). At last in SAS the current density can reach 1 MA/cm^2, and the main processes are TRAPATT-like ionization waves accompanied with powerful impact ionization and the carrier drift at saturated velocity in high electric fields (apparently similar processes might take place in the elements included in Kentech generators). We will see below that the same and even higher level of the current densities (up to 10 MA/cm^2) is characteristic of high-current/high-speed mode of the avalanche transistors considered here. Detailed mechanisms of the carrier transport and impact ionization will be discussed below.

An avalanche transistor was first mentioned by Miller & Ebers [14], see Fig. 2(A), and a simple model is presented at http://en.wikipedia.org/wiki/Avalanche_transistor. In a typical NPN common-emitter avalanche transistor circuit the base-emitter PN junction is forward-biased. Most of the electrons injected from the emitter diffuse (or drift) through the thin base and reach the collector region. In a space-charge collector region with a high electric field, electrons (both diffused electrons from the emitter and thermally generated electrons in the n_0 region) may gain enough kinetic energy to perform an impact ionization event in which a new electron-hole (e-h) pair will appear, as shown in Fig. 1. Two electrons are then swept into the n^+ sub-collector, while the hole that has been generated penetrates into the base and causes the injection of an additional electron from the emitter. This electron has a chance to generate a new e-h pair in the collector, and thus positive feedback between electron injection and the impact generation of holes takes place. This mechanism, which has been known since the 1950s, causes switching between the initial V_0 biasing and the V_{ceo} voltage, see Fig. 2 and figure caption. Due to the fairly high residual voltage

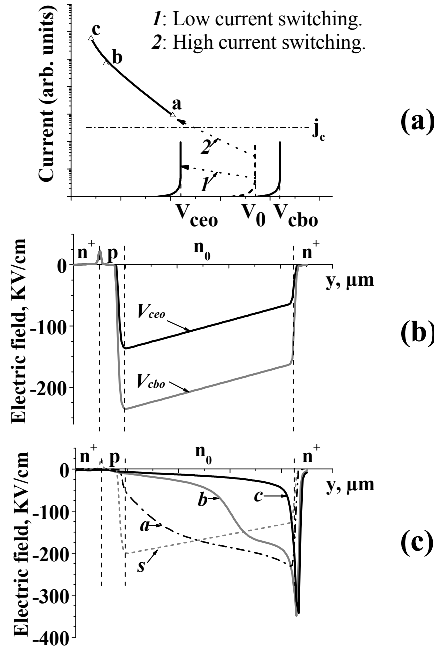

Fig. 2. (A)- Low current (1) and high current (2) switching scenarios of an avalanche bipolar junction transistor: the routes from an initial biasing state V_0 to a final quasi-steady-state are shown. Route (1) is related to switching when load resistance is so large, that density of injected electrons remains much lower than n_0- collector doping: corresponding electric field profiles are shown in (B). Route (2) is related to sufficiently low impedance, when the circuit allows the carrier density during the transient to exceed the doping significantly, resulting in drastic reconstruction in the electric field profiles (C). Profiles (a), (b) and (c) in (C) correspond to points a, b, c in (A). Depending on the circuit impedance, the final state will correspond to points *a*, *b*, *c* in (A) as the impedance is reduced. V_{cbo} is a collector-base breakdown voltage and V_{ceo} is a collector-emitter breakdown voltage with the base open. The first shows the absolute maximum for possible initial biasing of the transistor, while the second is the minimal residual voltage with low-current switching. Curve *s* in (C) shows the field profile at the initial biasing.

and moderate ionization rate, typical current amplitudes are low (≤1 A), the switching is slow (typically ≥100 ns for high-voltage structures) and this regime is not of interest for our applications. Under certain conditions, however, it may change to high-current-density/fast switching, or “secondary breakdown” as it was termed in the 1960s and 1970s, meaning that an additional mechanism may

be initiated after the first switching stage, resulting in a lower residual voltage than V_{ceo}. The "classical" interpretation of secondary breakdown given by Hower and Reddy [15] assumed a conical current distribution in n^+-p-n_0-n^+ and in n^+-n_0-n^+ structures, and this explanation remained popular until the recent results obtained using numerical modelling came to light [16–18]. The wonderful intuition of the authors of Ref. [15] allowed them to predict a high peak in the electric field at the n_0-n^+ boundary, which becomes a copious source of holes. This main feature of the "secondary breakdown" has been confirmed by the latest studies, but the reason given in the old classical model for why the peak in the electric field appears near the n_0-n^+ interface was later shown to be wrong [16–18]. This is certainly no fault on the part of the authors of the old work, Ref. [15], but a result of their limitation in principle to the only possible analytical approach available at that time: i.e. they had to assume that the electrons and holes were of constant (saturated) velocities and could not perform a rigorous solution to the problem with actual dependences of the electron and hole velocities over a broad range of electric fields. Consequently, they had to make the artificial assumption of a conical spreading of the current. It was later shown [16–18] that the peak in the electric field and the powerful impact generation of holes indeed appear at the n_0-n^+ boundary, but *this happens automatically in a one-dimensional manner* as a result of the difference between the electron and hole velocities over a broad range of fields (*not* caused by spontaneous current filamentation at the n_0-n^+ interface, and *not* associated with differences between electron and hole ionization rates, as claimed in [15]. Put briefly, according to Ref. [15] the peak in the electric field appears as a result of drastically increased current density near the n^+ sub-collector in the n_0 collector with respect to that near the p-base, while in reality (latest results) the electric field is forced out of the n_0-collector towards the n^+ sub-collector by an *electron-hole plasma region* formed near the p-base that grows across the collector. As a result practically the whole voltage across the transistor is now applied to a narrow, high-field, powerfully avalanching domain at the n_0-n^+ interface.

A qualitative schematic presentation of the differences between trivial low-current [14] and high-current [16–18] switchings is shown in Fig. 2, with brief comments given in the figure caption. Let the external circuit have a sufficiently low impedance (and /or the transistor operating area be sufficiently small), so that the trivial positive feedback in the avalanching transistor is allowed to increase the current density across the collector above the critical value of $j_c = q\ N_D\ v_s$ (where q is the electron charge $1.6{\times}10^{-19}$ C, N_D is the doping concentration in n_0

collector and v_s is the saturated electron velocity ~10^7 cm/s). Then the density of the electrons injected into the collector will exceed the charge of positive donors, and according to the Poisson equation the spatial derivation of the electric field (dE/dx) will change its sign (compare field profiles *s* and *a* in Fig. 2(C)). A significantly lower velocity of the holes with respect to that of the electrons over a broad range of electric fields will cause a kind of "trapping" of holes [17] which will then result in

1. formation of an e-h plasma region
2. its growth from the p-base/n_0 collector interface towards the n^+ sub-collector (compare field profiles *a*, *b* and *c* in Fig. 2(C))
3. shrinking of the collector domain (drastic reduction in the voltage across the transistor)
4. an increase in the ionizing field (and hole impact generation rate) at the n_0-n^+ interface
5. fast growth in the collector current.

This collector domain shrinkage, which drastically reduces the residual voltage across the switched-on transistor and thus allows a high current to be achieved, can be obtained only in n^+-p-n_0-n^+ transistors and not in those of the p^+-n-p_0-p^+ type [17, 18]. A common opinion emerged after the publication of [15], and remains popular among many scientists even today, that the reason why n^+-n_0-n^+ and n^+-p-n_0-n^+ are addicted to "secondary breakdown", while p^+-p_0-p^+ and p^+-n-p_0-p^+ are not is due to the predomination of the impact ionization coefficients of electrons over those of holes. It has recently been proved, however [16–18], that it is due to the difference in velocity between the electrons and holes, while the difference in ionization rates is of minor importance. This conclusion is significant not only theoretically, but also in practical terms, as it opens up a correct approach to the designing of avalanche switches based on materials other than Si. And last, but not least, the interchange between electron and hole velocities (υ_n and υ_p) in the simulations altered the behaviour of n-p-n transistors to that of p-n-p ones and vice versa, while the interchange between the ionization coefficients α_n and α_p had only a minor effect (of a few percent) on the exact residual voltage at the end of switching.

One can raise the interesting question of why within 3 decades nothing essential was done or understood regarding this problem from 1970 to 2001. Was it because avalanche transistors were not needed any longer? Actually no, as avalanche transistors were in use in various applications throughout that time and

new commercial transistor types even appeared. We believe that the reason lays in the fact that the necessary numerical methods and physical simulations did not exist in the 1970s, and that in the following years nobody returned to the problem from a physical point of view, assuming that it had been solved in 1970. As will be seen below, the use of modern simulators has allowed *a fairly comprehensive numerical model of an avalanche transistor to be created for the first time*, providing a very effective tool for achieving new developments in fast avalanche switches for solving some state-of-the-art problems in applications.

1.2 Operation of a Si avalanche transistor at high currents

Let us make a brief overview of the main features of the process as modelled in the quasi-static and transient one-dimensional and two-dimensional approaches with detailed comparison and excellent agreement with the experiment. The electric field profiles across the n_0-collector obtained in [17] as a result of quasi-steady state numerical modelling are shown in Fig. 3. Fairly illustrative are the reduction in the slope dE/dx (curves 1 and 2) as the negative charge of the injected electrons compensates for the charge of the donors, the change in the sign of dE/dx (curve 3) as the electron charge overcompensates for the donor charges and the collector domain shrinkage (curves 4–7) with spreading of the electron-hole plasma as the current grows. (Here electron current as a fraction of the total current is one parameter of the static model, and the shrinkage is more significant for a higher electron current fraction, which corresponds to later instants in the transient simulations). Finally, curve 8 shows what would happen if the electron velocity were lower than the hole velocity: the voltage across the transistor would remain high and effective switching would not be possible. This corresponds to situation of a p^+-n-p_0-p^+ transistor in which the carriers injected from the left are holes with low mobility (in Si), and thus a p^+-n-p_0-p^+ transistor cannot show

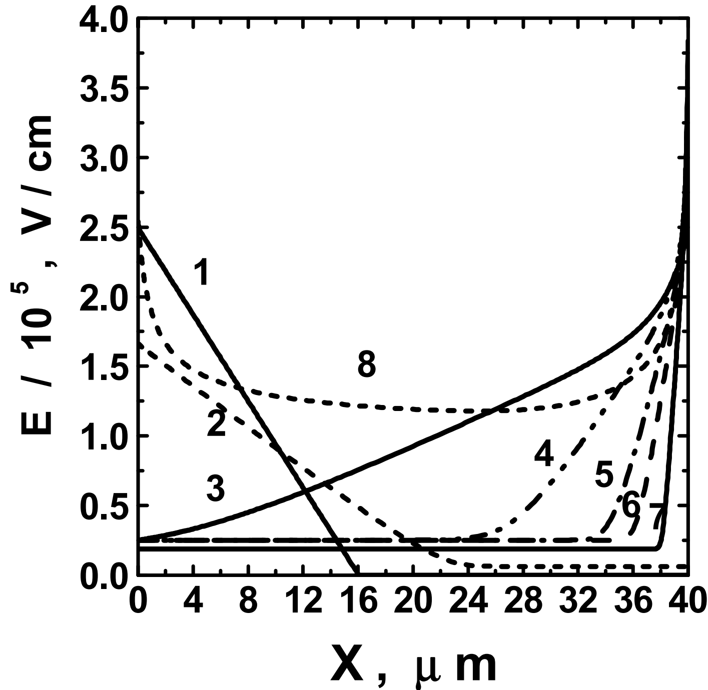

Fig. 3. Electric field distributions along the n_0 collector for various combinations of the injection current and total current J_{n0} (kA/cm^2)/J (kA/cm^2): 1—0/0, 2—0.85/0.856, 3—5/7.15, 4—12/18.6, 5—26/41.3, 6—40/64, 7—70/110, 8—40/81.1 [17, with kind permission from Elsevier].

"secondary breakdown" (effective switching) with collector field domain shrinkage and consequent drastic reduction in the residual voltage (as in curve 7). Qualitatively similar field profiles during the switching transient for different instants (corresponding to an increasing collector current), as seen in Fig. 4, were obtained in one-dimensional modelling, which included the external circuit with all its parasitics and the actual structure of a commercial ABJT FMMT417 [16]. These profiles may differ in detail from the static solutions, however, as the transient does not obligatorily reproduce all the intermediate steady-states of the static model. Fairly good agreement with the experiment was obtained in one-dimensional transient simulations (see Fig. 5), and even better agreement was achieved with two-dimensional transient modelling [18], in which very significant, avalanche-assisted current confinement was seen to takes place [Fig. 6] due to the electric field shrinking the holes *in the x-direction* [Fig. 7] and the resulting

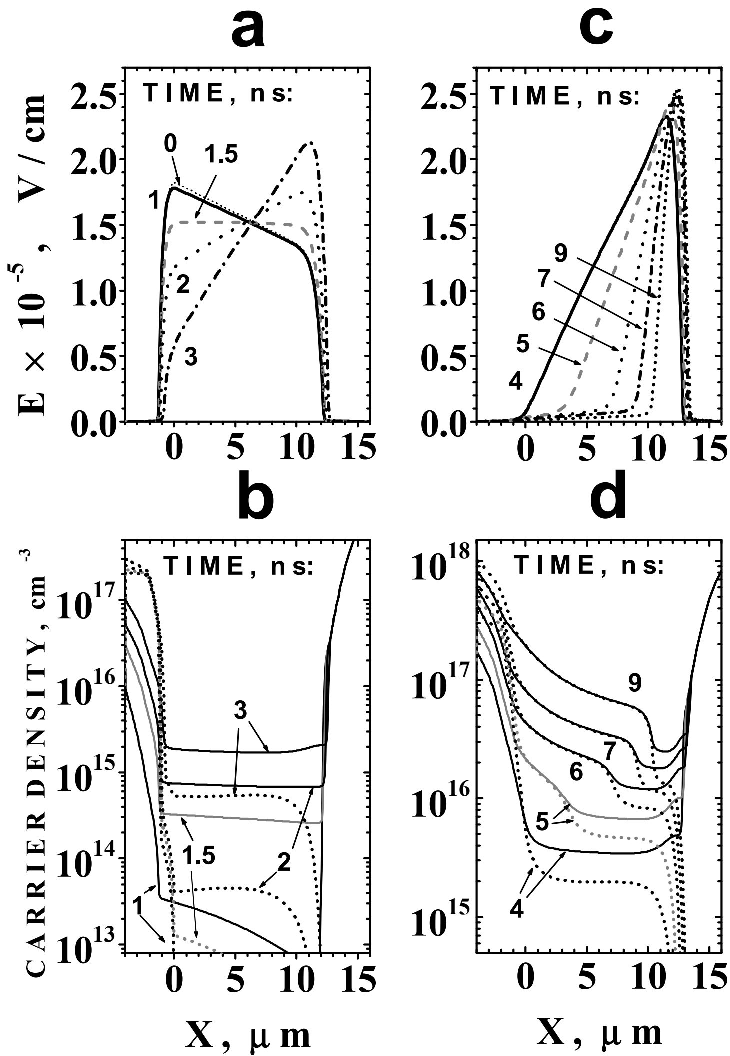

Fig. 4. (a), (c) Electric field and (b), (d) carrier density distributions across the p-base (x = - 4÷0 μm) and in the n-collector (x = 0÷16 μm) regions at various instants (t = 0÷9 ns). Electron (solid lines) and hole (dotted lines) concentrations are presented in (b) and (d), respectively. Time instants corresponding to the profiles with respect to the switching transient can be seen in Fig. 5(a) [16, with kind permission from IEEE].

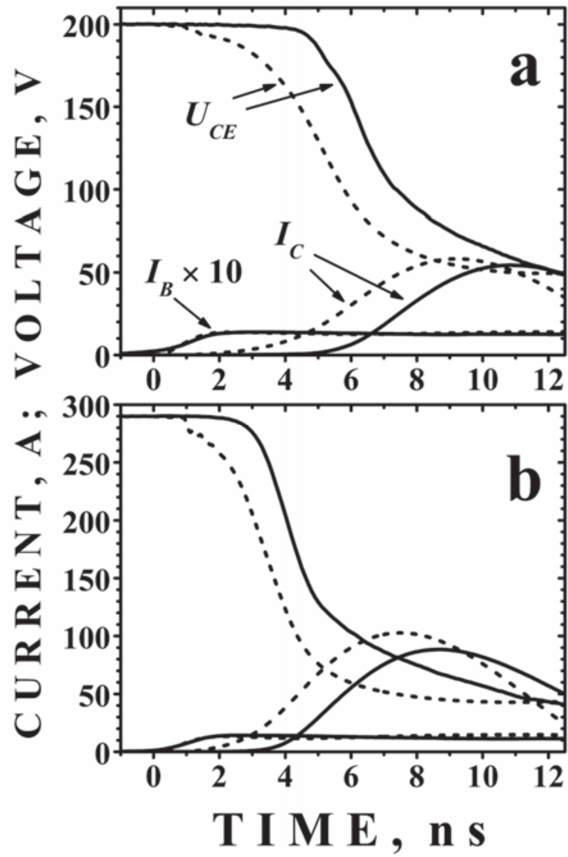

Fig. 5. Comparison of measured (solid lines) and simulated (dashed lines) current and voltage waveforms for two values of the initial bias voltage U (V): (a) 200 and (b) 290 [16, with kind permission from IEEE].

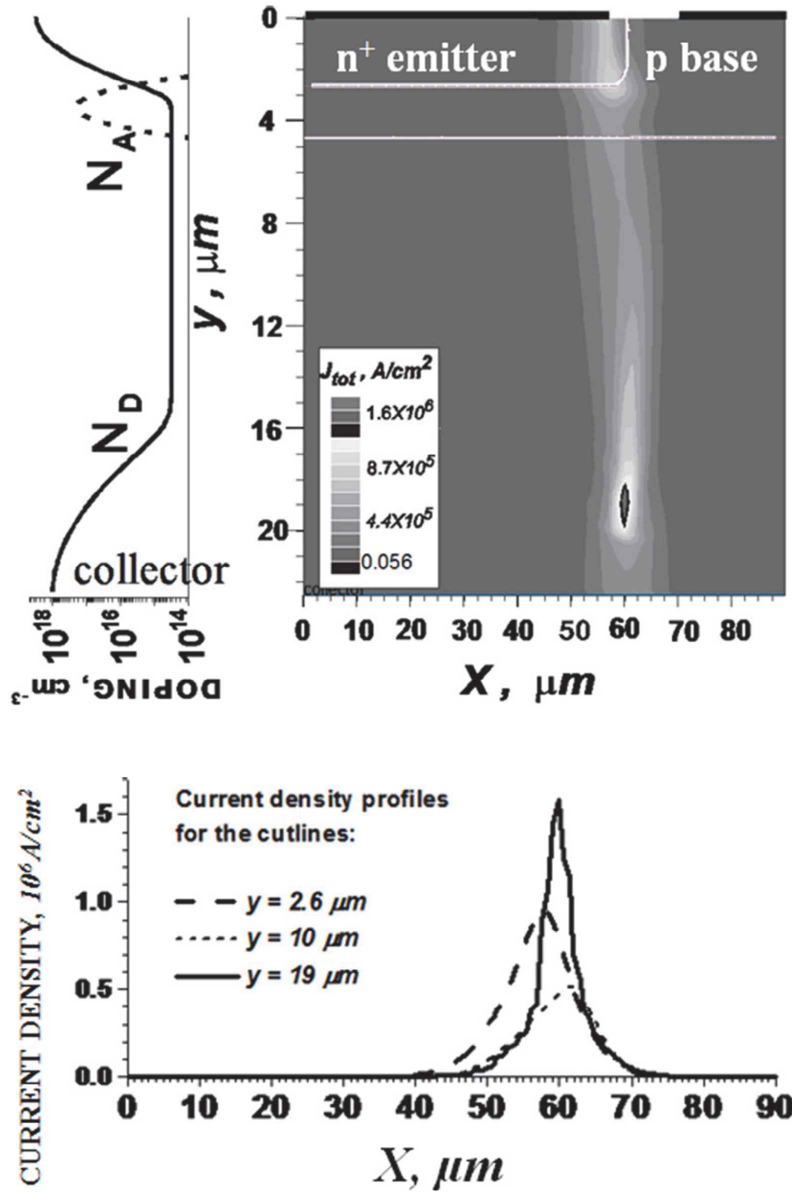

Fig. 6. Distribution of current density in the transistor at peak current. The geometry of the simulated device and the doping profiles are presented [18, with kind permission from IEEE].

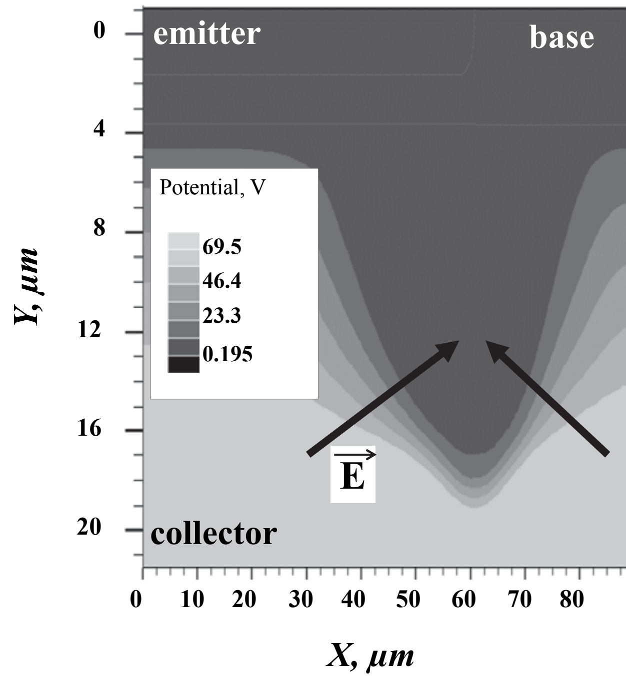

Fig. 7. Distribution of the potential at the instant t=8.4 ns, corresponding to the peak current [18, with kind permission from IEEE].

transverse current spread being much smaller than that typical of emitter current crowding without avalanching. The resulting time-dependent local heating (Fig. 8) must obligatorily be taken into account in the transistor reliability analyses.

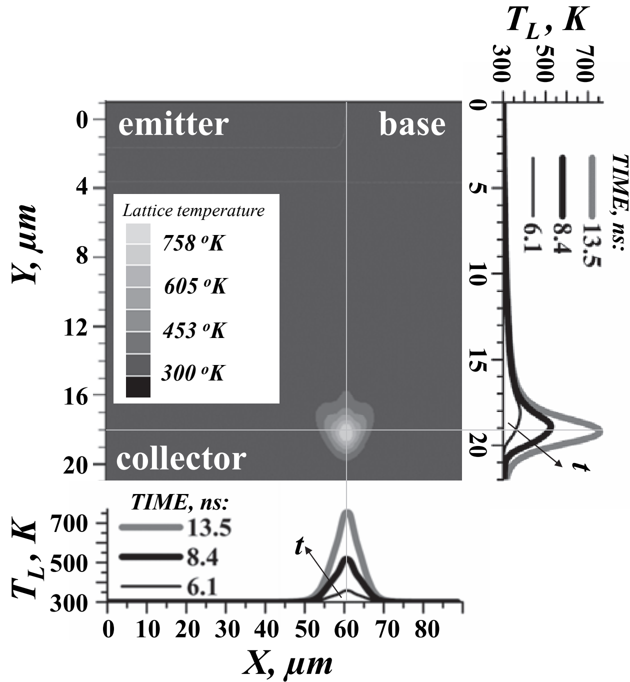

Fig. 8. Map of the lattice temperature at the end of the current pulse (13.5 ns), and both transverse and lateral temperature profiles at various instants [18, with kind permission from IEEE].

1.3 Advances in GaAs avalanche transistors at high currents

The fundamental conclusion discussed above, that high-speed, high-current switching ("secondary breakdown") is determined by differences in electron and hole velocities, leads to a simple rule for selecting the optimal semiconductor material for this operating mode: as high the electron mobility as possible, and *as high the ratio of electron to hole mobility as possible*. In this case the best candidate is not Si, but GaAs, with an expected ~1.5–2-fold gain in switching speed and efficiency. An experiment has shown, however, the *raising the switching speed by a factor of ~20* (!) [19] Furthermore, a proper selection of the transistor area has allowed the *circulating currents* to reduce the switching time to ~180 ps upon switching from 300 V to practically zero [20]. (This practically ideal, miniature, single-chip switch apparently has no competitor in the world, and its only disadvantage is that it is not commercially available and no stable

manufacturing technology has yet been properly developed). The phenomenon of superfast switching was explained by the generation of a comb of very unusual, ultra-high amplitude (~500–600 kV/cm), powerfully avalanching ("collapsing") domains narrowing in time down to nm-scale [21, 22], which appear as the result of negative differential mobility (NDM) in the electrons at extremely high fields (up to at least ~600 kV/cm) [23]. The evolution (generation and annihilation) of these collapsing field domains in dense electron-hole plasma causes fast current oscillations and the sub-THz emission [24] of extreme power density, which has a very high application potential in imaging and radars, particularly for quality control and security purposes. (This emission is not obtainable from Si ABJTs).

2 Motivation and goals

Two avalanche BJT switches (Si and GaAs) are both of practical interest, each in its own way. GaAs ABJT is incomparably faster and has higher efficiency, but its technology has not been properly settled, only a few laboratory samples are currently in existence in the world, and significant further efforts and investments will be required before this device can be made commercially available. On the other hand, the technology of Si BJTs is completely reliable and easily controllable, but various fundamental reasons do not allow Si ABJTs to compete with those of GaAs if the pulses shorter than ~2 ns are required to be generated, besides existing Si avalanche transistors cannot generate sub-nanosecond pulses at all. We will show, however, that much more advanced Si ABJTs can be developed provided the knowledge regarding their operating principles were drastically improved: Si avalanche transistors will certainly not reach the level of GaAs ABJTs, but a family of high-speed Si ABJTs can be designed for their operation in very important for applications sub-ns range.

Both Si and GaAs avalanche switches require significant improvements based on much better understanding of the limitations of their efficiency and reliability, while the main challenges for these two devices are different, and can be briefly formulated as follows.

1. The most important parameters of a Si ABJT are its switching speed (switching time) and efficiency (residual voltage). Our investigations have shown that both parameters can be significantly improved for a particular transistor structure once the current density during the transient has been increased. This may cause local thermal destruction of the transistor by the end of a single-pulse switching, however, and accordingly the structure and operation regime (circuit, etc.) have to be optimized with a view to this trade-off. This optimization will require a deep understanding of the three-dimensional transient in the transistor, which has been the main goal of the research reported here.
2. Unlike Si ABJTs, GaAs avalanche transistors demonstrates superfast switching independently on the thickness of their structure, thanks to the collapsing field domains, and optimization of the structural layers is not as important as in Si ABJTs. There is another challenge, however, that is of principal importance nowadays, namely the suppression of premature surface breakdown in the negatively-bevelled transistor mesa. This breakdown causes

a fundamental limitation, as an ABJT must operate near its bulk breakdown voltage, while premature breakdown does not allow proper biasing to be applied. Even the physical mechanism of surface breakdown has not been understood so far, and the methods of passivation known so far are not completely durable on account of the use of unduly thin sulphur films, while the physical mechanisms of passivation have not been interpreted in terms of impact ionization at the mesa surface. A new "soft" surface breakdown mechanism will be suggested here and validated by comparing numerical simulations with experimental data. Furthermore, an original method of chalcogenide glass passivation for GaAs mesa structures will be proposed in order to achieve complete suppression of premature surface breakdown and provide a plausible explanation for the physical mechanism supported by the numerical simulations and experiment.

2.1 The three-dimensional switching transient in a Si avalanche transistor

The approach developed in two-dimensional dynamic work [18] would allow comprehensive transient analyses to be performed for any kind of ABJT and the results to be reliable, *provided the switching size along the third coordinate (normal to the plane of Figs. 6, 7, 8) were known, were independent of the external circuit, and were to remain unchanged during the transient.* We will see, however, that this is not the case in many practically important situations. Moreover, we will see that the size of the switching region in the third direction not only affects device reliability and durability but may determine whether it is possible in principle to achieve short-pulsing switching, due to the effect of the size of the third coordinate on the current density, which in turn controls the switching speed (switching time) and efficiency (residual voltage). The competition between two important processes on the third coordinate will be introduced and analysed:

1. Transient current confinement (the "winner takes all" principle)
2. Current channel spreading.

We will see that the first one determines the possibility for increasing the switching speed, reducing the residual voltage and thereby increasing the current amplitude in a short-pulsing regime, *but* at the same time increasing the probability of thermal destruction of the device within a single pulse. The second

tendency works in exactly the opposite direction. *The chip layout in different transistor structures and the competition between these two tendencies in different circuits will lead to different results. It follows from our findings that smart designing of the layers of the transistor structure, the length (perimeter) of the emitter-base interface (“fingers”), and proper selection of the curvature at the corners of the “fingers” are obligatory for meeting the various application requirements for which a particular ABJT may have to be designed.* It will be shown in particular that the spatial inhomogeneities in the triggering current density controlled by the chip design allow special designs to be developed for high-current or short-pulsing switches, and even "universal" ABJTs capable of operating in both short and long-pulsing modes by virtue of their special three-dimensional dynamics.

2.2 Surface breakdown and passivation of the mesas of GaAs avalanche transistors

The second task of the work reported here was also associated with the reliability of high-speed ABJTs, but those based on GaAs.

The main problem with the reliability of both unique avalanching GaAs devices (the picosecond switch and the sub-THz emitter) currently concerns the very high risk of premature avalanche breakdown. Indeed, all ABJTs operate at a biasing which is very close to the volume breakdown voltage. The state-of-the-art diffusion technology and high-quality intrinsic SiO_2 dielectrics make it possible to fabricate guard rings in Si ABJTs, and thus the reliability problem for those devices with respect to surface breakdown has been solved.

Unlike the situation in GaAs BJTs (and HBTs), which have a relatively thick n_0-region, the guard ring fabrication technology for GaAs ABJTs is problematic, and the most obvious way of producing the necessary surface contour is deep mesa etching (up to ~60–80 μm). The transistor structure grown on a n+ substrate with the emitter on the top then becomes the only way of making a device with a p-base electrode (at least for high-voltage structures). Chemical etching to form a deep mesa provides a negatively bevelled contour for the p-base/n_0 collector junction (see Fig. 9c), and premature surface breakdown seems to be inevitable.

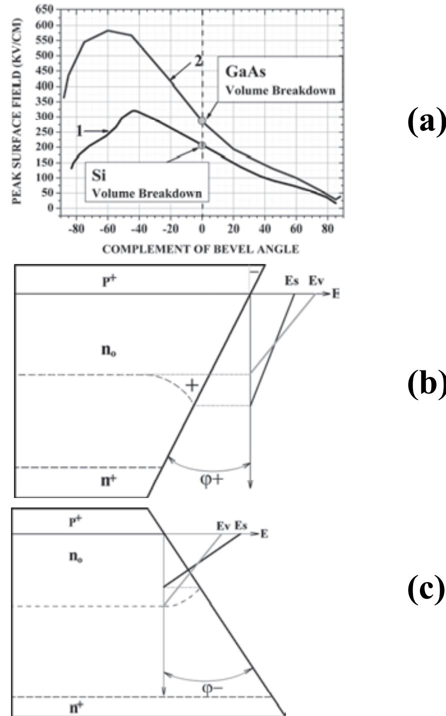

Fig. 9. Peak electric field at the surface of the p-n junction as a function of the angle of the bevelled mesa structure. Curve 1 in (a) is calculated in Davies & Gentry [25] for a Si p-n junction in the absence of impact ionization. (Here the value of the electric field at zero angle corresponds to the volume breakdown, and higher field values at negative angles represent an imaginary situation in which the volume breakdown voltage is applied to the structure while the impact ionization is absent.) Curve 2 in (a) was obtained in this work for a GaAs p-n junction using the "Atlas" device simulator (Silvaco Inc.) under the same presuppositions: the impact ionization is switched off and the electric field at zero angle corresponds to the peak electric field at volume breakdown. (b) and (c) show which bevel corresponds to positive angles, and which to negative angles. The electric field profiles inserted into (b) and (c) explain why the peak electric field at the surface (E_s) for a negative (positive) bevel angle is higher (lower) than that the peak volume (E_v). The thicknesses of the n_0 collector and p-base in the simulations were 42 and 5 μm, respectively, and the volume breakdown (breakdown at zero angle) was 470 V [IV, with kind permission from IEEE].

It is not clear from these speculations how in principle it would be possible to bias GaAs transistors close to the volume breakdown voltage in experiments. The actual answer is that premature surface breakdown always takes place, but for some reason there are favourable cases in which it has a “soft” character and does not destroy the device. This means that the surface breakdown current grows slowly as the applied voltage increases and in “good” samples it does not exceed the “dangerous” level of ~100 μA before sharp *bulk* breakdown occurs.

One should not mix up the surface breakdown, which occurs inside GaAs material in vicinity of the place where p-n junction touches the semiconductor surface with so called surface flashover that means the breakdown in the air near GaAs surface, but *outside* it. Surface flashover is a crucial issue to fast switches operating in high voltage (up to several kV, especially for the materials: silicon carbide, aluminum gallium nitride, gallium nitride, those have the breakdown electric field several times higher than that in GaAs). By first glance the surface flashover is unavoidable for most of the electronic devices as the breakdown electric field in the air (<100 kV/cm) can be from a factor of ~4 (Si) to 20 (SiC) smaller than the critical field typical of avalanche breakdown in the bulk of a semiconductor device. This is not always true, however, by the following reasons. First of all, the peak in the electric field at a semiconductor p-n junction near the surface has its maximum not on the semiconductor-air interface, but below the surface (inside the semiconductor) so that the peak in the electric field on the air interface is reduced. Then any avalanche breakdown requires initial carriers, which in flashover regime are typically considered to be emitted from the semiconductor and an efficiency of this process depend on different factors such as electrical properties of the surface, dV/dt rate of the applied voltage, etc. Various methods are known, which allow the suppression of surface flashover in the air, such as immersing the device to Fluorinert@ [26], integrated slant field plates and using high dielectric strength insulating encapsulation material [27]. A review of the mechanisms of surface flashover and the protection methods will not be given here, however, as the surface flashover is not known to be typical of our current objects (GaAs and Si p-n junction). One should bear in mind, however, that in broad-band materials such as SiC, AlN, GaN etc. this mechanism may become of principle importance in analyzing premature (and destructive) breakdown on the surface especially at sharp ramps of the voltage applied to p-n junction in reverse direction. Here we skip this broad topic thinking that it goes beyond the scope of the current study.

This does not mean that in our research we skip an approach of covering mesa-surface with a certain dielectric material, which would suppress the surface breakdown (this method is widely used not only in flashover, but also in a "traditional" surface breakdown inside a semiconductor material). It is termed passivation of the mesa surface (see details in the Discussions), which entails a further extremely challenging problem addressed in this thesis: that of finding a passivation method which will completely suppress premature surface breakdown in GaAs ABJTs and suggesting an appropriate physical interpretation for it.

3 The three-dimensional transient in Si avalanche transistors

The two-dimensional modelling performed in [17] showed excellent agreement with the measured voltage and current waveforms of a particular transistor (FMMT417, Zetex Semiconductors) in a particular circuit (C_0 = 2.2 nF, $R_L \approx 1\ \Omega$) on the assumption that the whole perimeter of the emitter-base interface (EBI) participated in the switching. This provided important and fairly reliable information on current crowding, electric field distribution and temperature mapping in the two-dimensional cross-section of the structure at any instant. At first glance this represents the final solution to the ABJT problem, providing a way of predicting the voltage and current waveforms for any circuit and transistor structure, and also for assessing device reliability with respect to its possible destruction because of local overheating. Moreover, this modelling should constitute a powerful tool for optimal transistor design to meet any particular requirement regarding the pulses to be obtained in different applications.

The question arises, however, of whether the numerical simulation actually provides a perfect description of the switching for any transistor structure, any chip design and any circuit.

Unfortunately not, as in many practically important cases, we observed very significant differences between the simulated and measured currents and voltages, differences which are certainly caused by three-dimensional effects, implying that different fractions of the emitter-base perimeter can participate in the switching depending on the conditions, and furthermore, the length of the perimeter participating in the switching can even vary in time (through self-organization) during the switching transient. Paper [I] introduces the problem of three-dimensional effects in Si ABJTS, show their practical importance and suggests three physical mechanisms which, together with the competition between them, determine a large variety of three-dimensional scenarios, depending on the circuit, transistor structure and design of emitter-base "fingers".

The first mechanism causes current crowding on the "winner takes all" principle. This principle as such is well known in different current filamentation phenomena, frequently those associated with impact ionization, but it has not been discussed earlier in connection with ABJT switching. The second and third mechanisms compete with the first one, i.e. increasing the length of the switching perimeter. The second mechanism, which was suggested in [I] and later confirmed by quasi-three-dimensional modelling [VII], we may call "fast turn-on

spread" along the emitter-base (e-b) interface. The process as such is analogous to the well-known turn-on spread in a thyristor. [In a thyristor the carriers from the switched-on region can penetrate laterally into an adjacent region and play the role of a current triggering switching in the second (so far non-switched) region. As a result, the switched-on area of the thyristor broadens in time.] There is a difference in principle, however, between the well-known turn-on spread in thyristors and its fast analogue in ABJTs suggested here. First, unlike the thyristor, in which switching may happen at a few volts on the anode, an ABJT can hardly switch on at voltages of less than ~1/3 of the maximum possible anode voltage, and thus turn-on spread can take place in an ABJT only during the initial switching stage, a point at which the turn-on spread in a thyristor *initiated by carrier transport in the p-base* is so slow ($\upsilon_{spread} < 1$ μm/ns) that similar spread velocities would not affect ABJT operation at all, as only an increase in this velocity by an order of magnitude is of practical interest. We will see in section (3.2) that such requirements can be satisfied in an ABJT, but only for spreading along the e-b interface at the beginning of the transient, a qualitative explanation for which was suggested in [I] and confirmed by three-dimensional modelling in [VI].

The third mechanism is based on competition between the "leader" and the remaining parts of the e-b perimeter, as described most clearly in [VII]. We will see below that two scenarios are possible at a sufficiently large capacitor value discharged across the transistor: current filamentation, causing local overheating and thermal destruction of the transistor, or relatively homogeneous switching of the whole e-b perimeter and reliable operation of the switch. Which of the scenarios will be realized depends on the magnitude of the initial inhomogeneity in electron injection along the e-b interface at the initial (triggering) stage. Moreover, we will see that a transistor with the same triggering inhomogeneity can be switched homogeneously in the long-pulsing/high-current mode and express non-homogeneous (but advanced!) switching in the short-pulsing mode due to a specific interaction between the current filament and the surrounding e-b perimeter [VII].

3.1 Experimental and simulation methods

Before we start discussing particular results of this work the research methods and methodological problems have to be briefly described.

Experimentally, observation of the emission caused by radiative carrier recombination would be the simplest direct method for characterizing the fraction of the e-b perimeter participating in switching. This emission can be seen through the gap in the e-b metallization (Fig. 10 (c)), but success in this particular

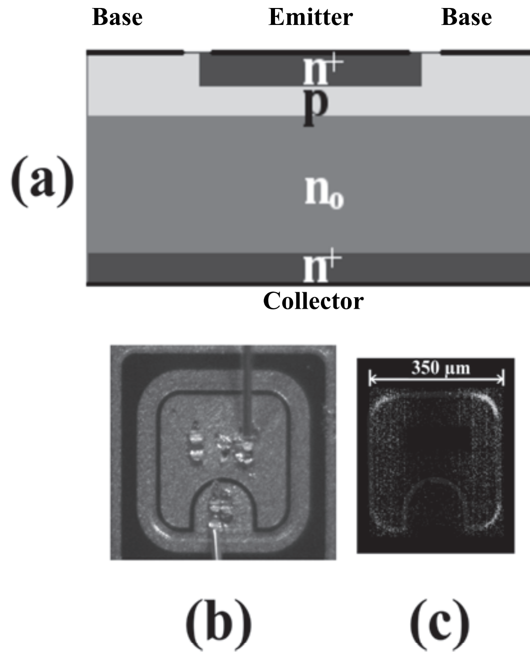

Fig. 10. The transistor structure cross-section (a), top view of the chip (b) and radiative pattern of the top of the transistor structure (c). The recombination radiation is seen in the gap between the emitter and the base ohmic contacts. The image is time-integrated at a repetition rate of transistor switching of ~50–100 kHz. It is unclear from this experiment whether the switching is realized in 3 (or 4) corners simultaneously, or in one corner every time, alternating for selection with the "coldest" corner each time [VI]. In any case the size of the switched-on region lies within the range ~80–250 µm, which is the accuracy of our knowledge of the short-pulsing operating perimeter. For brevity we denote this size below as ~100 µm [I, with kind permission from IEEE].

experiment is an exception which only became possible at a very high current density and high repetition rate. The problem lies in the very low efficiency of radiative recombination in Si, so that not only did a CCD camera fail to record the emission in most cases despite the very significant efforts undertaken to do so, but even sensitive up to wavelength of ~1.1 µm electro-optical converter, or MCP-

based high-speed image intensifier (LaVision), with a high sensitivity up to a wavelength of ~0.9 µm did not record the light. Further efforts were made to detect the switched-on region by transient measurements of the local potential in the metallization-free vicinity of the e-b p-n junction. Various modifications of a Kelvin probe were tried, but unfortunately all our attempts failed because of the oxide layer on the top of the Si at both the base and emitter surfaces, which we could not pinch through even with the hardest tungsten probes. Finally a very special arrangement, as shown in Fig. 11, was tried in which the oxidized Si layer

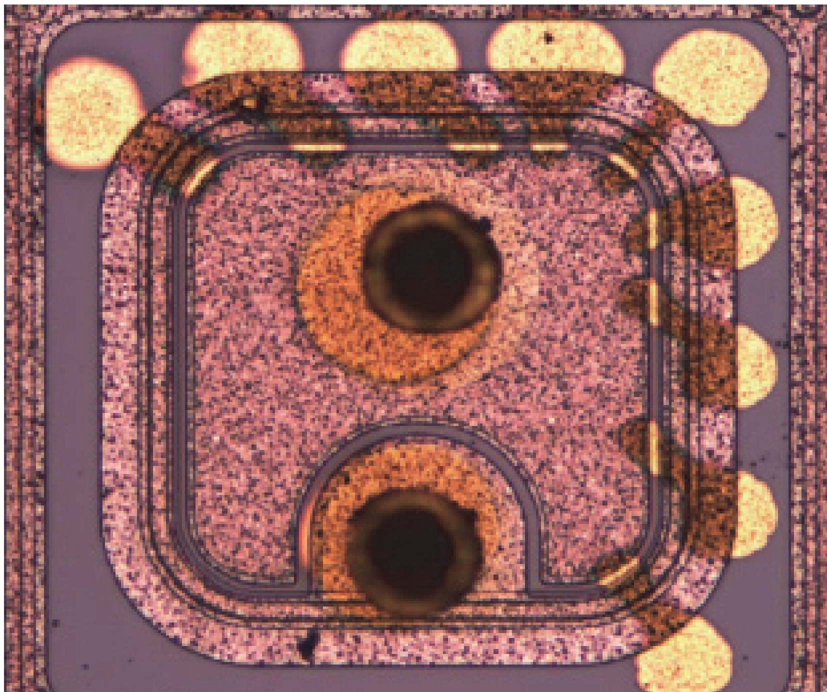

Fig. 11. Specially designed probing arrangement for evaluating the length of the switched-on perimeter during the transient.

was removed locally with an ion beam and replaced with miniature local metallization: each to be used as a probe for temporal/spatial potential profiles during the switching transient. Preliminary tests with only 3 probes showed that this arrangement was promising, but unfortunately the availability of assembly facilities did not allow us to employ this local probing method successfully with a sufficient number of probing patches.

All in all, we have obtained only one direct experimental measurement of the switched-on region, as shown in Fig. 10 (c). This means that in a general sense we can judge the size of the switched-on e-b perimeter only by comparing simulated and measured voltage and current waveforms: see, for example, Fig. 12 in [I].

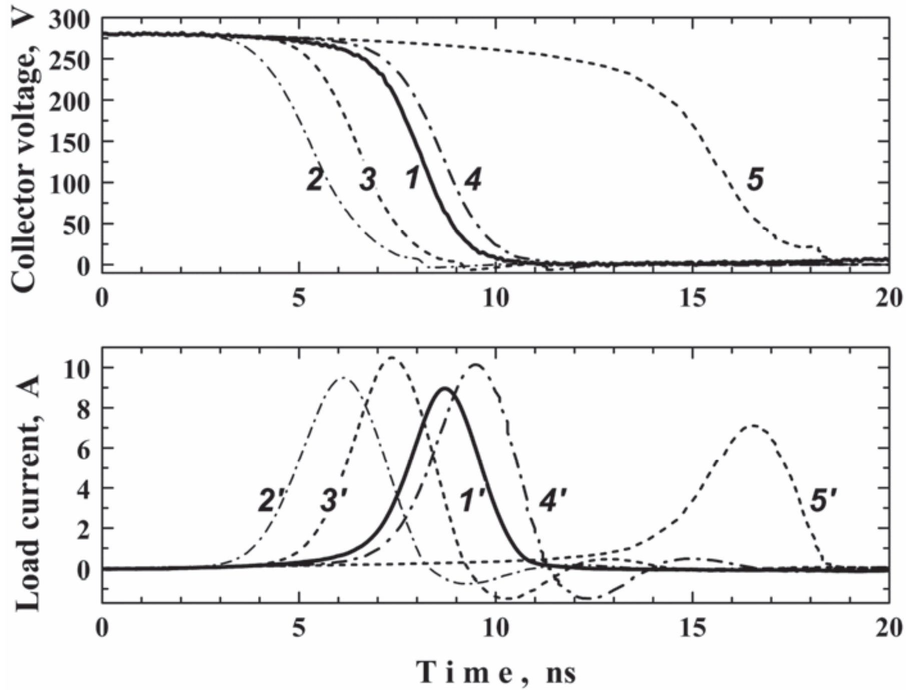

Fig. 12. Comparison the measured (1, 1′) and simulated (2-5; 2′-5′) collector voltage and current waveforms at different values of the effective (operating) emitter-base perimeter P_{eff} (μm): 2, 2′-20; 3, 3′-85; 4, 4′-200; 5, 5′-500. The zero time instant in the graph corresponds to the leading edge of the rectangular triggering pulse of amplitude 80 mA and duration 80 ns [I, with kind permission from IEEE].

This approach is the simplest one and fairly natural as long as we have to study three-dimensional phenomena using a two-dimensional simulator. In this case the effective e-b perimeter P_{eff} (the one participating in the switching) is a parameter of the model. This method is sufficient [I] as long as we are not dealing with time-dependent P_{eff} values during the switching transient. We will see later, however, that time-dependent P_{eff} is an actual situation controlling the operation of ABJTs in the general case.

Rigorous solution of the problem using numerical modelling requires *three-dimensional transient simulations* to be implemented with *external circuit included*. Unfortunately state-of-the-art device simulators do not allow this problem to be solved, as three-dimensional modelling cannot be combined with "MixedMode" operation of the ATLAS simulator (Silvaco Inc.), i.e. inclusion of an external circuit.

Thus the only option we have is to use a two-dimensional simulator in MixedMode and a "smart" quasi-three-dimensional approach which will allow the main features of three-dimensional switching to be analysed. This is not exactly equivalent to a rigorous three-dimensional solution, but it is the best that can be done, and fortunately it has allowed the main features of the process to be understood and a fairly good quantitative fit to the experimental data to be achieved in several important cases (thanks to moderate changes in switching size in the transverse direction, i.e. the X coordinate, see below, in the high-current switching stage).

Let us define coordinate X as a transverse coordinate parallel to the p-n junction plane and perpendicular to e-b interface in the top view (see Fig. 13(a)). Y is then the longitudinal coordinate in the direction of the current flux, and Z the lateral coordinate along the e-b interface in the top view (perpendicular to the plane of Fig. 13(a)).

Our "smart" approach consists of the replacement of Fig. 13(a) by Fig. 13(b). First a two-dimensional simulation of the transistor is performed (Fig. 13(a)) with the best guesses regarding the size of the effective perimeter P_{eff}. Then, from the cross-section in the X-Y plane we can find the characteristic size of the current crowding X_0 somewhere in the middle of fast transient stage. We then change the coordinate system. Y is still the direction of current flux, but X and Z are interchanged. In the new coordinate system we use a fixed structure size of X_0 in the direction perpendicular to the e-b interface Fig. 13(b) and the two-dimensional simulator calculates the transient in the Y-X plane, in which X is now the

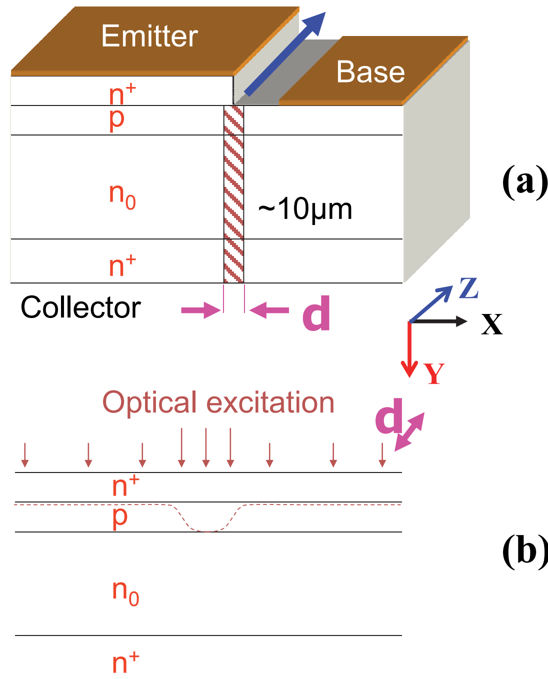

Fig. 13. A two-dimensional device simulator adapted for solving three-dimensional problems. (a) Three-dimensional view of the transistor structure cross-section. The value in the Z direction is set as a scale factor in the two-dimensional simulator. (b) Structure cross-section along the perimeter of the emitter-base interface (Y-Z plane in (a)), as used in the quasi-three-dimensional simulations.

direction along the e-b interface in the top view. Here a question immediately arises of how triggering can be effected in a system where the base electrode is absent. For triggering we use the optical excitation option in ATLAS, selecting the maximum intensity of the optical triggering signal in such a way that the switching delay in the simulated transistor corresponds to that in the experiment. The profile of light intensity L(X) in each particular simulation is selected in accordance with the problem to be analysed, but in any case the results obtained with Gaussian L(X) profiles of varying width are the most instructive [VI, VII].

3.2 Analyses of the simulation results

The method described above was used in [II, VI, VII] for studying the competition between the three mechanisms:

1. "Winner takes all"
2. Turn-on spread
3. Competition between switching of the "leader" and surrounding (larger) part of the structure at different degrees of triggering inhomogeneity along the e-b perimeter.

The practical need for considering this three-dimensional problem was shown in the earlier paper [I], the experimental data from which are taken as a criterion for the success of the interpretations given in the later papers (mainly [VI, VII]).

We will concentrate here on the main results and general logic connecting the papers devoted to the problem. Clear evidence that the same transistor has two effective perimeter lengths for different discharging capacitors is given in [I]. Namely, with a large capacitor (2.2 nF) a high-current (~80 A), long (~7 ns) pulse is generated by the transistor and the entire e-b perimeter of the transistor chip (1.6 mm) participates in the switching. With a small capacitor (82 pF) a ~10 A/2 ns current pulse is generated and the transistor itself selects an operating (effective) perimeter length of ~100 μm. This self-organization of the switching perimeter depending on the value of capacitor C_0, together with the mechanisms responsible for this behaviour are the main physical objects of interest in the current work.

Attribution of the shrinkage in the operating perimeter in the short-pulsing (10 A/2 ns) mode to the "winner takes all" principle is common to all the papers, while the details of this mechanism become more and more advanced starting from [I], progressing through [VI] and culminating in [VII]. The reason for the particular value of P_{eff}~100 μm selected by the transistor was not explained in [I], but was later interpreted in [VI] as the outcome of competition between the operating perimeter shrinkage, down to ~10 μm, and the turn-on spread, up to ~80 μm: see Fig. 14 taken from [VI]. It is also shown in [VII] that in short-pulsing (10 A/2 ns/82 pF) mode, even in a fairly homogeneous structure, a narrow filament (of ~10 μm at a minimum) forms upon complete quenching of the switching in the entire perimeter, which is the most pronounced illustration of the "winner takes all" principle.

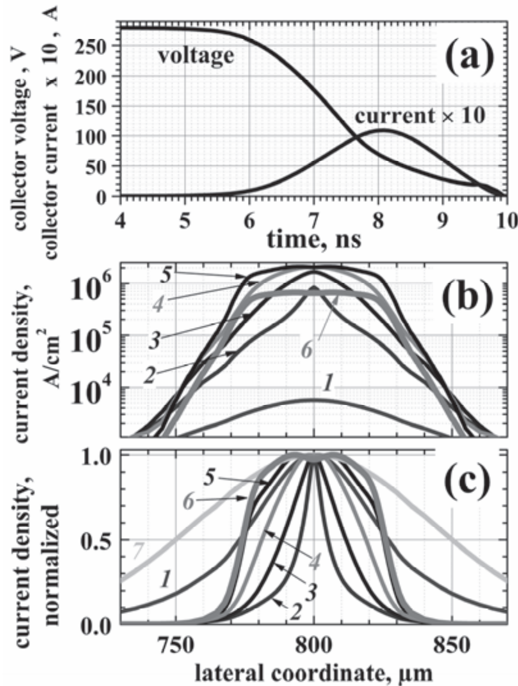

Fig. 14. Switching transient (a), current density profiles (b) and normalized current density profiles (c) simulated for an avalanche transistor with the same structure and the same circuit as that used in the experiments in Ref. [I] (capacitor value 82 pF). Instants corresponding to the curves in (b) and (c) are related to the transient in (a) as follows: 1-4.2 ns; 2-6.2 ns; 3-6.8 ns; 4-7.3 ns; 5-8.4 ns; 6-9.3 ns. Curve 7 in (c) shows the shape of the optical excitation. Note that the normalized curves in (b) first shrink from the initial excitation profile (curve 7) to current density profiles 1 and 2, and then spread to profiles 3, 4, 5 and 6 [VI, with kind permission from AIP].

We should emphasize again how the main puzzle that emerged in paper [I] was later resolved in [VII]. The question was: why does the same transistor survive in long-pulsing mode (entire perimeter in operation) and yet provide current filamentation in short-pulsing mode? At first glance, if it provides filamentation at 82 pF, then the current density in the filament will continue growing at a large capacitance of 2.2 nF and the transistor will burn out (as in the "2-transistor model"). Conversely, if the structure and triggering are very homogenous along the perimeter and homogeneous switching allows the switch to survive at long pulses, why does it provide filamentation at short pulses?

To resolve this puzzle we had to perform modelling according to the quasi-three-dimensional approach, which required the light intensity L(X) to be specified. If a characteristic width ΔX of the increased excitation near a corner of the chip (see Fig. 10(b), (c)) is more or less clear (~80 μm), the amplitude of the triggering inhomogeneity near this corner requires special comments. Let us make a plausible assumption that due to the curvature near the corners a crowding of the current injected from the emitter electrons (which trigger avalanche switching) should take place, so that the triggering inhomogeneity factor can be defined as $\alpha = (J_{n\ corner} - J_{n0}) / J_{n0}$, where J_{n0} is the triggering electron current density beyond the corner, and $J_{n\ corner}$ is that at the corner. Rigorous solution of the problem is not a simple task, as it requires rigorous three-dimensional transient modelling, but we can estimate the value of α by assuming the simple geometrical ratio $\alpha \sim \Delta_{eb}/R \approx 5\%$, where $\Delta_{eb} \approx 2.5$ μm is the distance between the base metallization and the e-b junction and R ≈ 50 μm is the curvature radius of the p-n junction at the surface (see Fig. 10(b)). The value α is used as a parameter in the model, but it is useful to keep in mind the inhomogeneity value α ~ 5% for the transistor used in the experiment.

Now a clear answer to the quasi-three-dimensional modelling problem [VII] consists of the following. Filamentation takes place in short-pulsing mode (82 pF/10 A/2 ns) due to the very effective quenching of the avalanching throughout the perimeter brought about by the slightly earlier switching at the corner. The point is that the electric field in the switching channel near the corner will already have been reconstructed while that in the surrounding regions has not. Then a reduction in the collector voltage due to discharging of the small capacitor stops the avalanching in non-reconstructed field domain (the entire perimeter except for the corners), while switching continues in the reconstructed domain, i.e. the corners (compare curves 3, 4 and 5 in Fig. 15: (a)- electric field at the corner, (b)- electric field between the corners, and (c)- total current density). This explains why a moderate inhomogeneity, α ~ 5%, is sufficient to cause the leading "corner" area to quench the switching in the remaining part of the transistor perimeter.

A schematic illustration of possible scenarios for the competition between the "winner" (the corners) and the rest of the perimeter is shown in Fig. 16. Here W denotes the switching transient at the corner where the switching acceleration started earlier. L1 shows the switching in the rest of the perimeter, fast switching having started later here due to lower current density. L1 corresponds to the

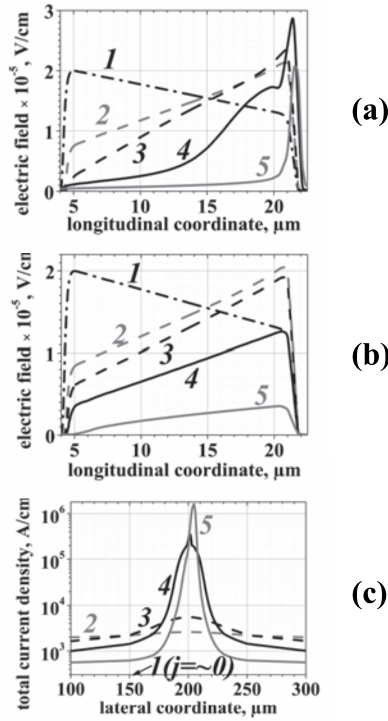

Fig. 15. Longitudinal (y) profile of the electric field in short-pulsing mode (a)- at the corners of the emitter-base interface (see Fig. 10(b, c)) and (b)- between the corners, and (c)- lateral (x) profiles of the total current density. The transient instants are: 1- 0.01 ns; 2 -8.09 ns; 3 -11.51 ns; 4 -14.4 ns; 5 -16.09 ns. The current reaches its peak value at 15.7 ns [VII, with kind permission from AIP].

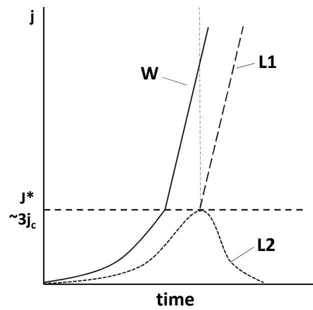

Fig. 16. Mechanism of the competition between the corner area (W) and the area between the corners (L1, L2 depending on the scenario assumed).

trivial case in which a delay in the switching acceleration causes a lag in current density growth. This is the case of a large capacitance (2.2 nF/90 A/7 ns), when the transistor survives provided that the triggering inhomogeneity has a moderate value ($\alpha \leq 5\%$). (Due to the large capacitance, the switch-on corner area does not discharge the capacitor significantly, so that the reduction in the transistor voltage V_{ce} does not quench the switching along the entire perimeter. At a low capacitance (~80 pF) the scenario follows curve L2, which means that earlier switching at the corners (W) quenches the switching in the entire perimeter except for the corners (L2) due to the mechanism illustrated in Fig. 15.

4 Surface breakdown and passivation in GaAs avalanche transistors

The second task addressed in this thesis is also associated with the reliability of a high-speed ABJT, but one based on GaAs.

In view of the very significant advances in GaAs ABJTs as unique sub-ns/ps range switches [20], for which no analogous devices exist in the world, and as high-application potential sub-THz emitters [24] providing extreme power density for quality control and security applications, as discussed at the end of the introduction, the solving of the main reliability problem affecting this device becomes a timely and critically important issue. As already mentioned, the negatively bevelled mesa should reduce the surface breakdown voltage to well below the bulk breakdown level, and it is critically important to study the mechanism of this surface breakdown in detail and to find a way for the transistor to be biased close to the bulk breakdown voltage. This is the last problem to be addressed in this thesis, but an extremely challenging one: to find a passivation method that permits premature breakdown to be completely suppressed in GaAs ABJTs (with a negatively bevelled contour of the p-base/n_0-collector junction) and to provide a physical interpretation of its mode of functioning. Formulations and solutions for the "soft" surface breakdown and passivation problems involved in the steady-state approach are provided in two papers [IV, V], and have been published at an international conference [28]. As stated in the Introduction, a chip of a GaAs bipolar junction transistor grown on an n^+ substrate inevitably uses a mesa with a negatively bevelled angle of the voltage-blocking p-base - n_0-collector junction, and surface breakdown voltage in this transistor must be significantly lower than the breakdown voltage in the bulk (see Fig. 17(a) taken from [V]). This is not acceptable for applications, however, as an avalanche BJT has to work in the vicinity of its bulk breakdown voltage. Our simulations of surface breakdown with a bevel contour analogous to the experimental mesas have shown *sharp* surface breakdown at a half of the voltage required for bulk breakdown (~220 V as opposed to ~470 V), see curve 3 in Fig. 18. This contradicted the experimental findings, as an attempt to exceed the surface breakdown voltage in the simulations would have already caused unlimited growth in the current at voltages below ~230 V, while in the experiment the surface current was increased gradually and in "good" samples did not exceed ~100 μA at voltages of ~450–460 V (see curve 1 in Fig. 18). We had concluded

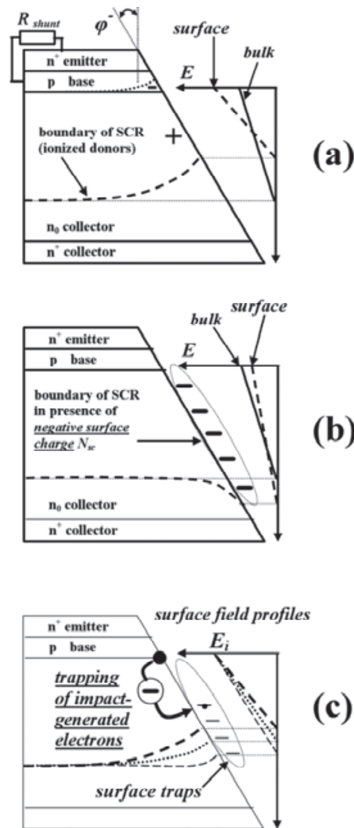

Fig. 17. Illustrations of (a) premature surface breakdown caused by narrowing of the space-charge region (SCR) on the mesa surface intrinsic to a negative bevelled angle (φ-); (b) suppression of surface breakdown by a negative charge N_{sc} on the mesa surface due to SCR broadening; (c) "soft" surface breakdown caused by the trapping of impact-generated electrons on the surface. This last-mentioned mechanism sustains surface breakdown over a broad collector voltage range, although limiting the surface current to a moderate (non-destructive) level [V, with kind permission from AIP].

that only negative charging of the surface states illustrated in Fig. 17(b) could increase the surface breakdown voltage, but the modelling including negatively charged surface states demonstrated *sharp breakdown* at elevated voltages, the extent of which was dependent on the density of the surface charge (see curves 4–7 in Fig. 18). A *gradual rise* in the surface current, similar to that observed in the experiment, was obtained when *surface traps* were introduced into the

simulations, in order to *trap the negative charge of the impact-generated electrons* due to surface breakdown (see an illustration in Fig. 17(c)). This physical mechanism for "soft" breakdown has never been considered before, and

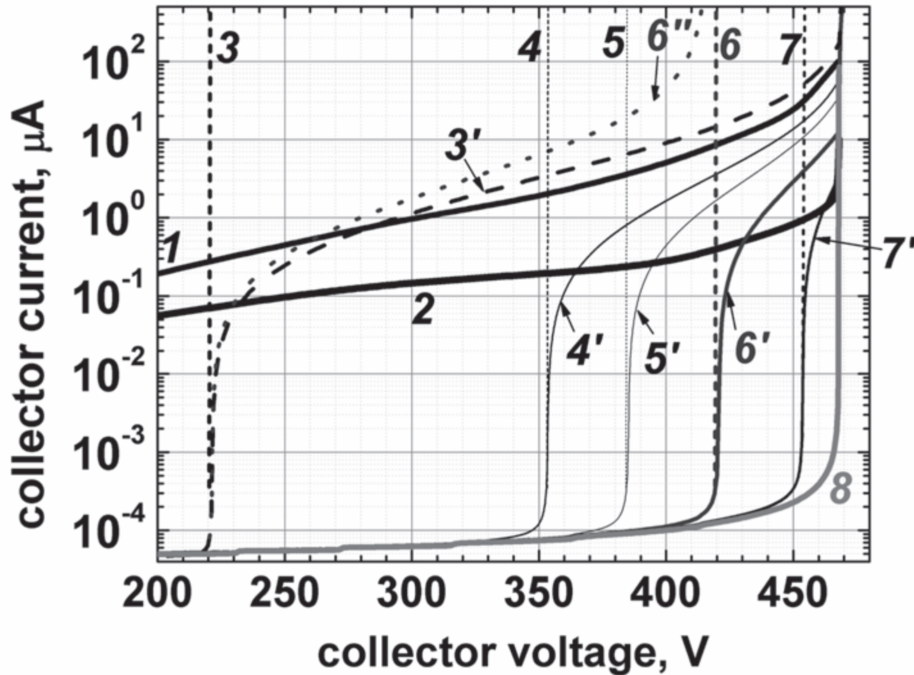

Fig. 18. I-V characteristics measured for one of the transistors with a shunted base-emitter [see Fig. 17(a)] before (curve 1) and after (curve 2) passivation, and modelling results obtained under various conditions. Curves 3-8 were obtained in simulations of different densities of the surface charge N_{sc} [cm^{-2}]: 3-0, 4-5 × 10^{11}, 5-6 × 10^{11}, 6-7 × 10^{11}, 7-8 × 10^{11}, 8-9 × 10^{11} (see Fig. 17(b)), where the last value provides a surface breakdown voltage (468 V) equal to that in the bulk. Curve 3' was obtained without any fixed charge on the surface (N_{sc} = 0) but with acceptor traps (N_T) having the same density (N_T = 9×10^{11} cm^{-2}) [see Fig. 17(c)], which permitted volume breakdown in the case of a fixed surface charge (see curve 8). Curves 4'-7' correspond to the same surface charge densities (N_{sc}) as for curves 4-7 but with surface traps added in the modelling: N_T = 9 × 10^{11} cm^{-2} - N_{sc}. This condition allows the "sharp" branch of the surface breakdown to be reached at the same collector voltage, 468V: compare curves 4'-7'. Finally, curve 6" shows the I-V characteristic at N_{sc} = 0 and N_T = 7 × 10^{11} cm^{-2} (compare with the reverse situation N_{sc} = 7 × 10^{11} cm^{-2} and N_T = 0 for curve 6') [V, with kind permission from AIP].

the first physical interpretation of it was apparently that published in paper [IV]. (It is worth noting that between the 1960s and 1980s, when the problem of surface breakdown in high-voltage junctions was a "hot topic" in device technology, there were no means in existence for investigating the mechanism in question, as only two-dimensional physics-based device simulators can be used for analysing it, and they were introduced commercially less than 20 years ago.) Furthermore, a combination of charged surface states and traps allowed plausible scenarios to be suggested for a large variety of I-V "trajectories" observed for different samples, and these could be related to surface breakdown with good degree of fit (see curves 1 and 3' in Fig. 18) between the experimental data and the numerical simulations [IV].

An experimental fact that deposition of the chalcogenide glass on the mesa-surface suppressed the surface breakdown completely we attributed to a large density of negative surface charge formed on the surface (see Fig.17 (b); curves 4'-7' and 8 in Fig.18) associated with intrinsic of the chalcogenide glass properties of U-centers (see Fig. 19). The methodology used here has provided an original

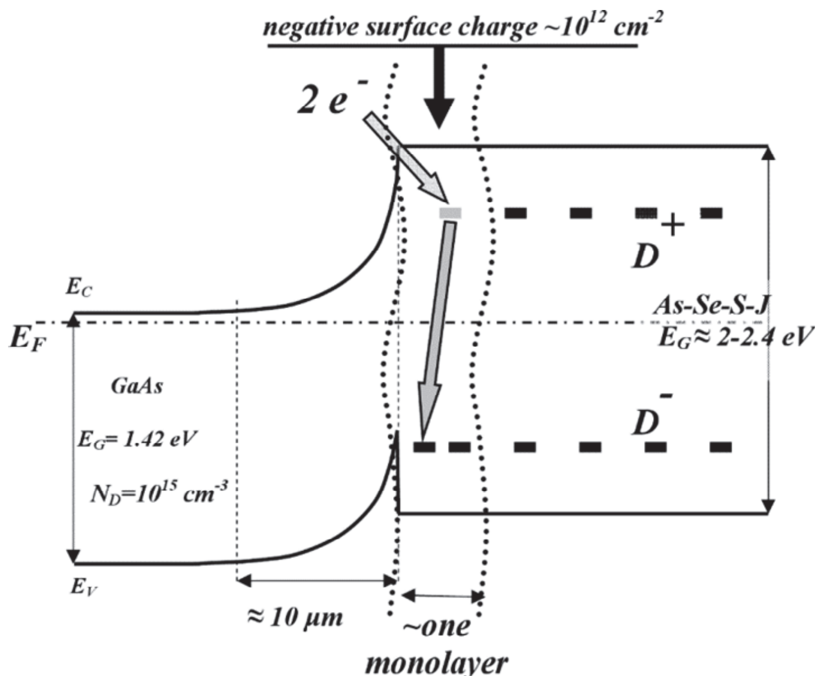

Fig. 19. Schematic presentation of the band diagram for the GaAs / chalcogenide glass interface [V, with kind permission from AIP].

approach to the passivation problem [29, 30], which was concerned with various chemical reactions on the semiconductor surface but never employed physical modelling to study the effect of surface charges on device operation. We think that our approach to the interpretation of the passivation effect on surface breakdown is a more robust (less speculative) one than those adopted before [29, 30].

5 Discussions

5.1 The three-dimensional switching transient in a Si avalanche transistor

The main achievements made in avalanche bipolar transistor switching in *high-current mode* can be attributed first to publications that appeared in the 1960s and 1970s [15, 31–35], and then to papers produced during the last ten years, mainly in the Electronics Laboratory of the University of Oulu [16–18]. An obvious question then arises: does this mean that there were no publications on avalanche transistors in the meantime, and if there were, why they are not included in the above considerations and referred to in the appropriate places. The reply to this question is the following.

1. Ordinary (low-current, low-speed) avalanche switching was understood and properly characterized in the 1950s and lies beyond the scope of the present work.
2. High-current switching ("secondary breakdown") was the subject of hot discussions in the 1960s and 1970s, in addition to which the publication of reference [15] seemed to put a "final" end to the problem, at least with respect to the analytical approach, which was the only possible one at that time. It is important to note, however, that the problem of avalanche switching is too complicated for a rigorous analytical solution, and the model suggested by [15] used artificial quasi-three-dimensional assumptions which led to erroneous conclusions that could be resolved only using forms of numerical modelling that have been introduced within the last decade [10, 16–18].
3. Several groups of publications devoted to avalanche transistor switching appeared during the interval 1955–2012, and these can be classified as follows:

   a) Engineering publications that did not concentrate on the physical mechanisms of avalanche transistor operation, but dealt rather with advanced parameters of pulsers for different applications [2, 36–39]. These papers are not considered here as they bear no direct relation to our subject.
   b) Publications dealing with fairly advanced approaches of compact modelling, including various 2-D and even 3-D features of relatively fast

avalanche transients in low-voltage ABJTs [8, 40, 41]. These all belong to the "ordinary" low-current operation mode, however, as simple estimates show that in their case the density of the injected carriers does not exceed the donor doping in the collector. This is a sufficient reason for us to ignore all the papers in this group.

c) Finally, there are publications [42, 43] in which the reconstructed collector field domain is considered, this being intrinsic to high-current switching. Qualitatively correct static 1-D profiles can be derived from these considerations based on a certain analytical approach, although this cannot be considered useful, instructive or even correct. The point is that even impact ionization was not considered in those models (!), and removal of the electric field from the base-collector p-n junction obviously cannot be justified, as this would prevent generation of the holes and formation of the electron-hole plasma. Thus this last group lies outside the scope of our interest as well.

Only numerical consideration of the problem allowed us finally to get good description of high-current ("secondary breakdown") switching mode [16–18] and excellent fit to the experiment has finally been obtained using 2-D transient numerical modeling. This model for a Si ABJT is *completely deterministic* and it works perfectly provided that the size of the *operating* perimeter of the emitter fingers is exactly and correctly known. (*Only one tunable parameter* is the injection coefficient of the electrons across the emitter-base junction at moderate currents, but this one affects only switching delay and cannot explain drastic differences in the current and voltage waveforms recoded in the experiment). It was clearly shown in [I] that the only possible way of interpreting drastic differences of the transistor operation in short- and long-pulsing modes is associated with variation in the operating perimeter, and later on it was found [VI, VII] that the only possibility of fitting all experimental observations to possible physical mechanisms consists in temporal variation of the operating perimeter during the transient. Thus a correct description of the experimental observations in a broad range of the pulse durations and amplitudes cannot be achieved without account of 3-D transient processes.

The methodology of the current work has permitted so far to give systematic explanation of the experimental data obtained *only for one commercial avalanche transistor type* FMMT-417 (Zetex Semiconductors Inc.) *in a broad range of pulse amplitude and durations*, however. Further verification of correctness of this

approach for large variety of the transistor structures and chip configurations require large work to be performed in cooperation with the device manufactures, which requires very significant efforts, funds, and participants involved. The suggested methodology and main operation modes should be generally correct, however, as they utilize rigorous approaches to physics-based device modeling. The main roughness consists in using quasi-3-D approach (due to limitation of the computers and simulators to model rigorous 3-D transient including external circuit).

We think that this approach can give semi-quantitative predictions for different structures, chips and circuitry. A success in application this tool to optimal designing of a new generation of high-speed (sub-nanosecond) avalanche switches requires well-developed intuition of researchers involved and an experience in study of this interesting and complicated device.

In summary, we believe that correct, rigorous solutions to the one-dimensional and two-dimensional dynamic problems concerning an avalanche transistor at high current have so far been presented only in papers [10, 16–18], and that the *three-dimensional problem has apparently been addressed using a physics-based modelling approach for the first time in this thesis (and related papers) and thus this work cannot be compared with other publications*. The approach used here could even be considered a rigorous one, if we ignore the *quasi*-three-dimensional nature of the approach and a certain roughness in the selection of the inhomogeneity parameter α.

5.2 Surface breakdown and passivation of mesas in GaAs avalanche transistors

Strange as it may seem, the physical reason for "soft" surface breakdown has been unknown until now. Indeed, the problem of surface breakdown in relatively high-voltage (up to ~10^3 V) GaAs p-n junctions first appeared only in the 1970s, when epitaxial methods allowed non-compensated doping to be achieved in GaAs layers below 10^{15} cm^{-3} [44]. The problem has not been properly solved, however, as high-voltage GaAs bipolar devices were unable to withstand competition from Si at that time, so that insufficient "laboratory" efforts were made to investigate surface breakdown at high-voltage (more than 100 V) GaAs p-n junctions. The breakdown problem has been under consideration up to now largely in connection with photodiodes utilizing the Schottky barrier to GaAs [45], or multiple layers based on various III-V materials [46, 47]. The reason why it was not addressed

was evidently that the making of a guard ring by ion implantation at a relatively shallow depth (≤4 μm [45]) was possible in these fairly thin structures (≤ 3 μm) at breakdown voltages below 100 V, or else passivation (see below) was used [48]. Surface breakdown in III-V-based semiconductor devices was the focus of interest mainly in the case of field-effect transistors [49, 50], which have a completely different geometry from the high-voltage p-n junctions considered here. Some avalanche photodiodes based on III-V and SiC [51–53] have positive bevel angles when mesa etching is used (it is scarcely possible to produce positive bevel angles in BJTs), and in addition the surface is always passivated. Thus *all the surface breakdown scenarios discussed in the literature differ essentially from those intrinsic to a high-voltage GaAs BJT*, since interest in the latter has been limited for many years. [To the best of our knowledge no plausible model was suggested at all for interpreting "soft" surface breakdown despite the fact that it is fairly commonly observed at high-voltage GaAs p-n junctions (see detailed discussions in [IV])]. After the introduction of miniature pulsed sub-THz emitters [24] and unique electrical switches [20] operating at room temperature the situation altered, allowing the *solving of the problem of "soft" surface breakdown to become the fairly challenging task of this work.*

A supplementary task (or alternative route) would have been surface passivation aimed at premature surface breakdown suppression even in a negatively bevelled mesa. Despite the fairly extensive literature on this topic, earlier findings were not of any help in solving our problem. Indeed, the surface passivation problem in small-dimension GaAs-based structures was addressed in connection with the low current gain in GaAs-based heterojunction bipolar transistors (HBTs) [54, 55] rather than in conjunction with breakdown. One fairly popular method in recent decades (~500 papers) has been chalcogenide thin film deposition (see review [30] and references therein), and this method is still in use [48, 50]. Unfortunately, the promising improvements in the characteristics of various devices (FETs, APDs, Schottky diodes, etc.) achieved with a large variety of chalcogenide passivation technologies [30] did not prove durable, due to degradation of the thin films (~0.5–1.5 nm).

Thus the practical achievements of thin-film chalcogenide passivation technologies are questionable with respect to film durability, and the chalcogenide glass passivation method suggested here may provide a more practical solution to the problem.

Another important question is the physical mechanism of the passivation which causes an increase in the surface breakdown voltage. Despite detailed

discussions of various electron processes involving the hanging bounds on the surface [30], the methods employed earlier did not deal with the electric field distribution, carrier transport or impact ionization at the surface, the last-mentioned being without doubt the main subject to be considered in order to obtain an interpretation of the breakdown phenomena. From this point of view, the methodology presented in the present work establishes an “original” approach to the passivation problem, one which we have not found in the literature.

We have no means so far to confirm it for large variety of different GaAs p-n junctions with negatively beveled mesas as they are not available. We made our conclusions based on a certain group of GaAs BJTs experimental samples specially designed, manufactured, and existing in our laboratory and we think that suggested here mechanism can be of importance for other bipolar structures and semiconductor materials provided their surface contain high density of traps.

6 Conclusions

6.1 The three-dimensional switching transient in a Si avalanche transistor

Let us summarize the main stages in our study of three-dimensional effects in a Si ABJT and the results obtained. As already discussed, the task was a really complicated one, and it is hardly realistic to expect a rigorous solution for any particular case using the available modelling tools.

As a first approach we used a two-dimensional, two-transistor model, and we have to confess that we are not satisfied with the results of this approach. The second model was a quasi-three-dimensional one employing an inhomogeneity parameter which does not change with time and does not depend on the C_0 value. This parameter is $\alpha \approx (j_{max} - j_{min}) / j_{min}$, where j_{max} and j_{min} are maximal and minimal current densities of the electrons injected in the base and reaching the n_0 collector along the e-b interface). In reality the factor α can be time-dependent, and the assumption of a fixed switching size in a direction perpendicular to the e-b interface in the horizontal plain (Z) similarly does not allow us to claim that we have achieved a precise quantitative solution to the problem. We have, however, managed to answer all the questions regarding the three-dimensional dynamics that were raised by the experiment, as even the quantitatively obtained voltage and current waveforms are fairly close to the experimental ones, and thus the following main conclusions can be formulated:

1. The size of the switched-on length of the perimeter of an avalanche transistor does not obligatorily coincide with the technological length, but will vary in time and depends on the initial voltage, the circuit and the triggering current density and its lateral variations.
2. The switched-on region at the initial switching stage tends to show filamentation of a minimal size comparable with the n_0-collector thickness, which can be prevented by a counteractive turn-on spread mechanism. The competition between these effects determines the actual (time-dependent) size of the switching region, which in turn determines the switching speed, efficiency, device reliability and the shape of the current and voltage waveforms.
3. Various scenarios are possible for the temporal dependence of the switching size on the transistor chip design and the triggering level, but the

understanding of the three-dimensional dynamics that we have achieved allows a reasonably smart transistor design to be proposed for obtaining the required parameters and ensuring controllable and reproducible operation.

4. In particular, a transistor design that introduces controllable triggering inhomogeneities will permit the realization of both short-pulsing and long-pulsing modes with the same transistor type.
5. The quasi-three-dimensional approach using a two-dimensional simulator suggested here allows in principle the modelling of different transistor designs and circuits, and consequently reasonably accurate prediction of the switch parameters.

6.1.1 Future prospects for research and development in this field

It is worth noting the importance of this topic for future applications. Various interesting findings were made during the years spent on this modelling which give a clear vision of how a new generation of high-speed (sub-nanosecond) silicon avalanche transistors could be designed and fabricated. (*There are no transistors of this kind currently on the market*). This work was based on the understanding that fast, effective switching has to be realized on the basis of an extreme current density which nevertheless does not cause thermal destruction. In some cases described in this work the 3-D effects help us to attain this main goal, while at other times the transistor "resists" the achieving of extreme current densities. All of this will have to be accounted for in the smart designing of a new generation of fast avalanche transistors.

Successful experimental realization of this challenging task (with commercial prospects) will require direct access to Si BJT technology, including complete structure and chip design information. We hope that this work will be done in the future and we will be able within a reasonable time to suggest a series of ABJTs optimized for a variety of ns and sub-ns applications with current amplitudes not achievable using any other commercial Si devices. One example of the unique parameters predicted for special Si ABJTs can be found in paper [III] (4 A / 1 ns / 10 MHz). This may be a surprise for many researchers and engineers, but we believe that the development of ABJTs has been "blind" so far, as designers have not had an appropriate tool for optimal ABJT design, and have scarcely had the necessary deep understanding of the operation of this interesting and complicated device.

6.2 Surface breakdown and passivation of the mesas of GaAs avalanche transistors

Both the newly suggested passivation method [V] and the charging of traps by means of impact-generated electrons are critically important for superfast switches and sub-THz emitters, as biasing voltage limitation and possible instability in the surface current together determine the reliability of these devices. Surface breakdown and passivation mechanisms may therefore be of major importance not only for GaAs but also for other compound semiconductor materials with a high density of surface states (e.g. GaN, AlN, etc.), and not only for BJTs but also for HBTs and HEMTs. Finally, the traps controlling surface breakdown require a certain time to become charged by impact-generated electrons, and this may critically affect device reliability with respect to achieving an acceptable dU/dt rate for the voltage applied to the device. This could mean that the surface breakdown voltage may depend drastically on the speed of the voltage source, biasing the device towards high-repetition-rate regimes. Thus the reliability of a device may depend in a fairly sophisticated way on the circuitry used in the applications.

6.2.1 Future prospects for this research

So far only *static* tasks have been considered for impact-generated electron trapping at the surface, while a much more complicated and fairly important issue concerns solution of the transient task in a manner that takes into consideration the various parameters of the trapping centres, such as the capture cross-section, the carrier lifetime of the traps, etc. Solving this task could provide a comparison between the modelling and the experiment that could prove very convincing for the ascertainment of the nature of the mechanism involved and lead to important practical recommendations associated with the ability of the surface breakdown phenomenon to withstand the dU/dt effect (apparently reducing the actual breakdown voltage in the dynamic mode). Indeed, if we imagine that the collector voltage can grow so fast between two switching events that the impact-generated electrons fail to provide a sufficient charge on the traps during this short time, it would imply that the surface current associated with avalanche multiplication would start to grow earlier (at lower voltages) than with a slow rise in voltage. This would limit the maximum repetition rate which transistor is able to withstand, and this question certainly deserves detailed investigation.

Fortunately, these limitations are not related to passivated surfaces, where the surface charge is determined by the GaAs-chalcogenide glass interface and does not require impact ionization.

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