A 14.6 GHz – 19.2 GHz Digitally Controlled Injection Locked Frequency Doubler in 45 nm SOI CMOS

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***Abstract*— In this paper we present a wide locking range (14.6 GHz – 19.2 GHz and 12.65 GHz – 20.6 GHz, -3 db and -6 dB, respectively) injection locked frequency doubler implemented with 45 nm CMOS SOI technology. The doubler is designed and optimized for a 5G sliding-IF transceiver architecture. It exploits a digitally tunable LC tank to enhance the frequency range. Measured results show 36 – 55 dBc fundamental and 40 – 54 dBc 3rd harmonic suppression as well as 10 dB peak conversion gain. Phase noise performance of the doubler has also been measured. The power consumption varies from 5 mW to 11 mW. The core size is 270 µm x 450 µm.**

***Keywords*— 5G, frequency doubler, injection locked, LC oscillator**

I. Introduction

Frequency multipliers are widely used in transceiver circuits and radar systems. Several frequency doublers operating on the Ku- and K-band frequency range have been presented in the literature. Frequency multipliers can be divided into three categories: mixer-based, device nonlinearity based and injection locked oscillator based. The first one suffers from complex mixing of harmonics and relatively poor power consumption. Doublers based on amplifying the harmonic distortion resulting from device nonlinearity [1]–[4] often employ transformer baluns to achieve wide operating range and suppression of the fundamental and unwanted harmonic components. This suppression is, however, difficult to achieve due to the imbalance in the transformer resulting from parasitic capacitances between the coils and the fundamental rejection is typically only around 35 dB [1]. One design uses a hybrid coupler to achieve fully balanced operation that achieves 44 dB fundamental rejection but has a narrow tuning range [5].

The injection locked frequency doubler (ILFD) principle uses an active doubler consisting of a differential pair with shorted drain nodes. This inherently cancels the fundamental, injects even harmonics into the loop and locks the oscillation frequency at twice the input frequency [6]. With this topology, balanced operation is achieved without transformer components. Injection-locked oscillators are particularly suitable for phased array transceivers due to their excellent phase noise performance [7]. The phase noise of the output of the multiplier is ideally $20log_{10}(n)$ dB higher than the phase noise of the input source, where n is the locked harmonic [8]. In the doubler case this results in a 6 dB phase noise degradation.

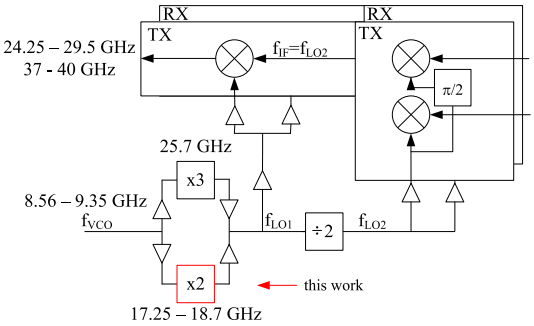

Fig. 1. Block diagram of the LO scheme in the sliding-IF transceiver.

Distributing the LO signal consumes a lot of power in beam-forming transceivers. One way of minimising this, and distributing gain to different frequencies, is to use a sliding-IF architecture, where LO side injection can be used in the mixers. The presented ILFD is intended to be part of LO generation block shown in Fig. 1. In the frequency planning one of the main constraints was to limit the frequency range of the external phased locked loop (PLL) to less than 1 GHz i.e. 8.56 – 9.35 GHz. This results only to ∼9% tuning range requirement of the VCO. The ILFD presented in this paper is designed for a dual-band sliding-IF phased array transceiver, where the output RF frequency range will be from 24.25 GHz to 29.5 GHz (bands n257 and n258) as well as 39 GHz (band n260). The doubler is designed to cover the lower bands where input VCO frequency and the IF frequency are on the same range and a separate tripler will cover band n260. At the moment we have measured results only from the doubler part, and rest of the paper concentrates on it.

II. Injection Locked Doubler Design

Injection locked frequency multipliers are designed to oscillate without input signal at a so-called self-oscillation or ”free-running” frequency, on which the LC tank is tuned. The circuit topology of the doubler is shown in Fig. 2. Input biasing, bias circuits for individual N- and P-side biasing (points V_a and V_b, respectively) and output buffers are not shown in order to improve readability.

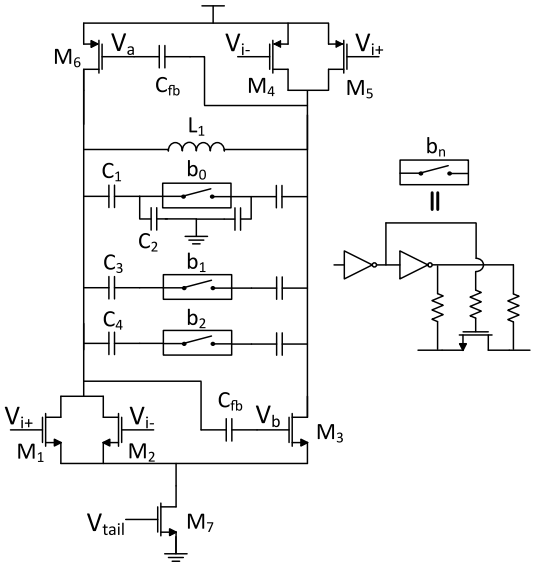

Fig. 2. Doubler schematic.

In injection locked oscillators, locking range can be extended by several means: reducing the oscillator quality factor (Q), increasing the injection current I_{inj} and reducing I_{osc} by reducing the the gm of the amplifier stage. The first technique results in less efficient operation and the last one in reduced oscillation amplitude or even loss of oscillation [7]. Achieving high Q for the LC tank is challenging due to poor Q-value of capacitors and varactors at high frequencies and therefore further Q degradation is often not necessary.

From power consumption perspective, tuning the free-running oscillation frequency is the best choice. The doubler design follows the basic topology as shown for example in [6]. In our circuit, no varactors are used, but a capacitor bank with switchable MIM capacitors with 3-bit control is implemented. The tank Q can be maintained high while still having a large locking range by having a capacitor bank with digital control. With this scheme, the continuous locking range of the doubler can be greatly extended if the individual locking ranges are overlapping.

The performance of the doubler can be optimized for certain frequencies since the conversion gain is peaking in the center point of the locking range which coincides with the free-running frequency. When all of the switches (W/L = 89.6 µm / 40 nm) are off, the oscillation frequency is determined by the series connection of the capacitances C1 and C2 of the b0 switch, which provides the highest oscillation frequency. This way, the "all switches off" oscillation frequency is controlled rather than determined by parasitic capacitances alone. Like in [6], locking range is further increased by attenuating the feedback signal with C_{fb}.

As the doubler is going to be the starting point of the LO path in the transceiver, full voltage swing at the output node is not necessary. On the contrary, the swing should be limited so that the following LO buffer amplifier stages after the doubler are not causing unnecessary distortion. The LO needs to be divided to several paths, i.e. mmW to IF and IF to BB mixers on both TX and RX paths. A capacitive attenuator consisting of a 75 fF MIM capacitor and the approx. 10 fF input capacitance of the first buffer stage provide a small attenuation for the signal. A second buffer stage is designed to drive a differential 100 ohm probe load.

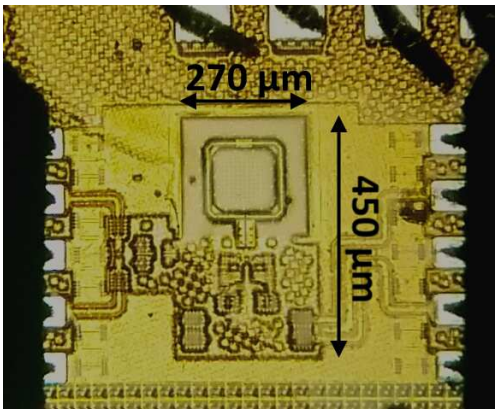

Fig. 3. Doubler chip micrograph.

III. Measurement Results

A micrograph of the doubler is shown in Fig. 3. The power consumption of the doubler core varies from 5 mW to 11 mW depending on the tunable tail bias setting. The first buffer consumes 4 mW and the second one 11 mW.

The measurement setup is shown in Fig. 4. The setup contains Cascade Microtech differential 67 GHz GSGSG probes, Marki Microwave BAL-0067 baluns and coaxial cables with 1.85 mm connectors. A Keysight PSG E8257C signal generator is used as the signal source and a Keysight N9040B UXA signal analyzer has been used in the spectrum, locking range and input sensitivity measurements. Keysight E4446a spectrum analyzer is used to measure the phase noise. Cable, connector and probes losses have been measured separately without the DUT and are removed from the presented results over the entire frequency range at input and at output separately. Due to probe setup, measurements were conducted in the room temperature only.

The doubler self-oscillation measured with all eight frequency settings is shown in Fig. 5. A typical spectrum result is shown in Fig. 6. The measurement has been conducted with -14 dBm input power and 8 GHz input signal. In the LO path, as the LO signal can be amplified to mixers with tuned amplifiers, fundamental leakage and higher order harmonics are further attenuated. Fundamental leakage varied from -30 dBc to -55 dBc in the measurements. The rejection of the odd harmonics depends on the amplitude and phase balance of the differential inputs, and is dominated by the response of the external input balun.

The -3 dB locking range has been measured by sweeping the spectrum with constant input power of 0 dBm between 7 GHz and 9.8 GHz. Fig. 7 shows the multiplied output with four out of eight different oscillation frequency control values.

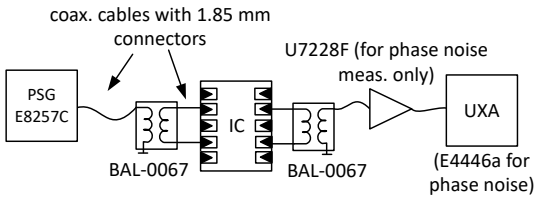

Fig. 4. Doubler measurement setup.

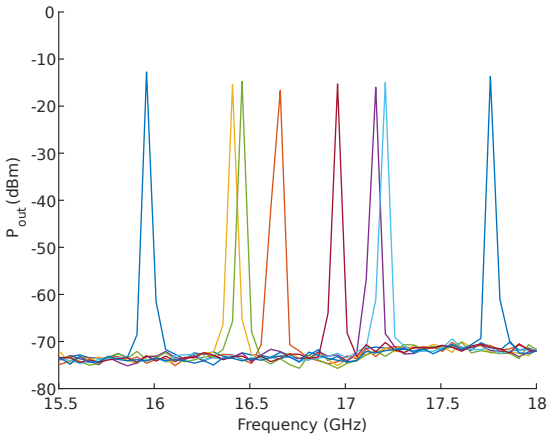

Fig. 5. Doubler self-oscillation frequencies for the eight center frequency settings.

-3 dB locking range is achieved from 14.6 GHz to 19.2 GHz. If the input power is increased to 2 dBm, the -3 dB locking range extends from 14 GHz to 19.6 GHz and -6 dB locking range from 12.65 GHz to 20.6 GHz. Thus, the 3-bit digital control expands the locking range 48% with good margin (overlap) between the controls.

The input sensitivity plot is shown in Fig. 8. The input power was reduced until the lock was lost and the last power level with lock was recorded. The measurement is shown on four of the frequency control values. As expected, conversion gain is at its highest near the free-running frequencies, where the peak conversion gain is approximately 10 dB. From Fig. 8 it can be also seen that the doubler can be operated over a wide

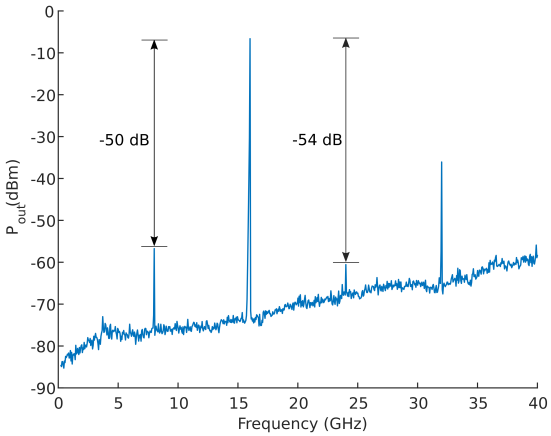

Fig. 6. Doubler spectrum measured at 16 GHz.

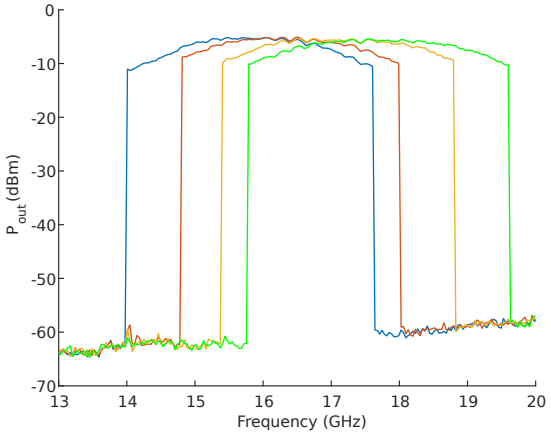

Fig. 7. Doubler locking range for oscillation frequency settings 0 (blue), 2, 5 and 7 (green).

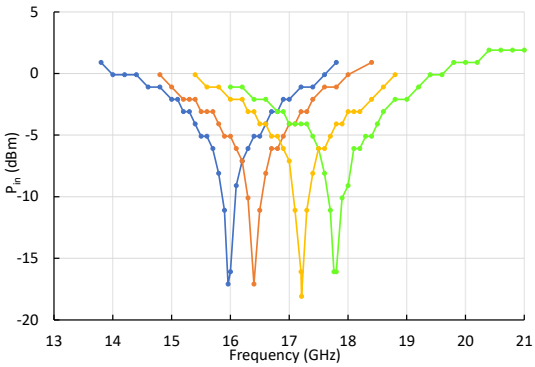

Fig. 8. Doubler input sensitivity measured with oscillation frequency settings 0 (blue), 2, 5 and 7 (green).

frequency range with lower input power level (-5 dBm) while still maintaining lock. This reduces the fundamental and 3rd harmonic level while still maintaining the frequency control range requirement of the multi-band system with good margin.

The measured phase noise at 18 GHz is shown in Fig. 9. The phase noise measurement is impacted by the purity of the signal source, the signal level at the doubler input and the signal level at the receiving phase noise measurement instrument input. For this reason, a buffer amplifier (Keysight U7228F) has been used to boost the signal level for the spectrum analyzer. The same amplifier is present in the signal generator phase noise measurement (lower plot) and the phase noise has been measured with the same 6 dBm power in both cases. The measured doubler phase noise is mostly approximately 6 dB higher than the signal generator phase noise that has been measured at 9 GHz.

The implemented doubler is compared against recent works in Table 1. It achieves state-of-the art performance with wide tuning range, low area, supply and power consumption demonstrating the benefits of digital control for also above 10 GHz solutions. The wide tuning range in [2] has been measured with high input power of 5 dBm and with that power level curves in Fig. 8 suggest also a major extension for locking range in our work.

Table 1. Comparison of frequency doublers operating at similar output frequency.

Reference	2010 [6]	2018 [5]	2014 [9]	2013 [2]	2010 [10]	**This work**
Process	130 nm CMOS	65 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm CMOS	45 nm CMOS SOI
Topology	ILFD (varactor)	push-push balanced	casc. stacked current reuse	single balanced	casc. stacked current reuse	ILFD (mimcap)
-3 dB tuning range (GHz)	12 – 14.2 (16.8%)	22.5 – 24.8 (9.7%)	20 – 24 (18.2%)	15 – 36 (82.4%)	18 – 26 (36.4%)	14.6 – 19.2 (27.2%)
Input power (dBm)	5	0	0	5	0	0
Output power (dBm)	-5	5	-5	-5	4	-5
Fund. suppression (dBc)	45 – 53	44	32 – 53.8	33	30 – 50	36 – 55
3rd harm. suppr. (dBc)	57	–	–	–	15 – 25	40 – 54
Supply voltage	1.3	1.2	2.6	1	2.6	1
Power dissipation (mW)	5.2	31.2	13.9	4 – 11	18.2 – 20.8	5 – 11
Area (mm^2)	0.083	0.35	0.57	0.32	0.29	0.12

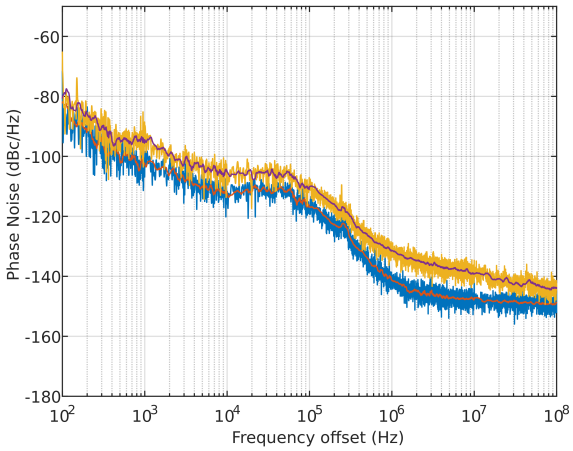

Fig. 9. Doubler phase noise measured at 18 GHz (yellow curve) compared to signal generator phase noise measured at 9 GHz (blue curve).

IV. Conclusion

The designed digitally controlled injection locked frequency doubler has a wide locking range while benefiting from the excellent phase noise performance inherent to injection locked multipliers. It can also operate with a relatively low input power level over a wide frequency range. The phase noise performance of the doubler has been demonstrated to be close to ideal with state-of-the-art fundamental and 3rd harmonic suppression. By using switchable MIM capacitors, locking range of the push-push injection locked doubler can be extended by 50%. Digital control with high-Q inductors and MIM capacitors enables to optimize the performance vs. tuning range with the on-resistance of the MOS switches even at frequencies above 10 GHz. The implemented doubler is capable of supporting wide bandwidth requirements of 5G mmW band solutions and can be further optimized for even wider tuning ranges by enhancing the digitally controlled capacitance matrix.

Acknowledgment

Nokia is acknowledged for financing the project, GlobalFoundries for chip processing and Keysight for providing measurement equipment. This work was supported in part by the Academy of Finland 6Genesis Flagship (grant no. 318927).

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