Noise Consideration of Radio Receivers Using Silicon Technologies Towards 6G Communication

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***Abstract*— Silicon technologies have been the dominant approach to implement radio frequency transceivers up to 5G systems with need for simplified antenna interface in large scale antenna arrays at mm wave region. Recent interests to achieve data rates up to 1 Tbps call for higher carrier frequencies to achieve sufficient bandwidth. Frequencies above 100~GHz will pose serious challenges to silicon based implementations as speed of the transistor in practical designs will not scale up similarly as typically expected in digital signal processing. It's impacting not only the achievable gain but also on noise of the transistor that directly scales up as a function of frequency impacting the link range. This paper presents specifically behaviour of noise parameter as a function of frequency in transistor level and in simulated low noise amplifiers using state-of-the-art CMOS SOI and SiGe BiCMOS technologies. It will be shown how noise parameter should be considered when evaluating achievable link ranges as a function of the frequency.**

I. Introduction

One of evident and largely discussed target for 6G communications is to achieve 0.1-1 Tbps data rates. In practice, that will require signal bandwidths in the range of tens of GHz or even more depending on the modulation used. Such spectrum could be only found at frequencies above 100 GHz even in case of massive MIMO due to many practical issues related to the implementation, properties of radio channel and availability of spectrum. Both high bandwidths and carrier frequencies are also more vulnerable to physical non-idealities. Therefore one should target for rather simple modulation that would also be more power efficient to transmit [1]. Simple modulation with low signal-to-noise (SNR) requirement will compensate for the loss per antenna element at very high frequencies but leads to lower spectral efficiency as a compromise. However, that is a sensible trade-off for any radio design when boundaries of implementation technologies are approached. A recent paper analyses achievable radio link ranges at 300 GHz with decent antenna gain and quite moderate noise figure for different scenarios [2]. However, it uses conventional approach with noise data from existing low noise amplifiers (LNAs) designs and output power from corresponding power amplifier (PA) publications. The approach is far from being generic and leads lacking understanding of the true scaling effects as a function of technology.

Speed of the transistor depends on the properties of a particular technology. Especially, at sub-mmWave/THz range, III-V semiconductors based technolgies such as gallium nitride (GaN) and indium phosphide (InP), have superior performance over silicon [3]. However, silicon germanium (SiGe) or complementary metal oxide silicon-on-insulator (CMOS SOI) technologies provide much better compatibility for large scale system integration even with complex digital circuitry. Therefore specific attention should be paid on the feasibility of these technologies before adopting more complex solutions with lower integration rate and thus larger form factor and difficult packaging. Transceivers operating in 150-240GHz region have been demonstrated using those [4], [5] where former depicts the integration of antenna elements on the same silicon die. Technology limits have been studied against state-of-the-art power amplifiers (PA) and their power delivery capability in the survey available in [6]. Similar studies are highly limited for LNAs [7] at the other end of the link.

This paper focuses on scaling of noise parameters and to some extend also gain as a function of frequency in LNAs with impacts on receiver and radio link performance estimation. Section II will focus on fundamental noise properties in silicon based technologies. Analysis is utilized for practical LNA design constraints and frequency scaling aspects in Sections III. The results are reflected to receiver design in Section IV with future work and conclusions in Sections V and VI, respectively.

II. Scalability of Noise parameters in SiGe HBTs and CMOS SOI

Noise of a receiver comprises of noise and gain of all the blocks in the receiver chain. However, as classical system noise formula by Friis (Equation 1) depicts, the first blocks noise dominates, taken that there is sufficient gain in the following blocks.

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_n - 1}{G_1 G_2 ... G_{n-1}} \quad (1)$$

The noise of each block is highly dependent on two contributors: the noise properties of the active devices i.e transistors and diodes and the losses of passive components such as interconnects and matching components. When operating the transistors far below the unity gain metrics (f_T and f_{max}), the gain of the stages is relatively high, meaning that the noise of the first stage of the receiver chain is dominant for overall noise figure. Operating closer to technology frequency limit, the gain quickly degrades forcing the designers to trade-off gain and noise at cost of power

dissipation as more gain stages are needed and the first stage gain is not enough to suppress the noise of following stages.

Intrinsic noise of transistors is sum of all noise sources which have been categorized on basis of their origin to thermal noise, shot noise, substrate noise and flicker or 1/f noise [8]. Overall minimum achievable noise for a *transistor* - luckily for system designers - has been simplified into models that are highly dependent on just the f_T of the transistor. Sze in (2) has included transistor resistances and transconductances [9] whereas Lee has used even more simplified form with a single constant in (3) [10].

$$F_{min} \approx 1 + K \cdot \frac{\omega_0}{\omega_T} \sqrt{g_m(R_g + R_i + R_s)} \tag{2}$$

$$F_{min} \approx 1 + 2.3 \frac{\omega_0}{\omega_T} \tag{3}$$

Gain depends on the process f_{max} for amplifiers with power gain such as power and low noise amplifiers and f_T for other amplifiers. On frequencies below unity gain frequencies, the current gain reduces 20dB per decade. Maximum stable power gain curves characterizing f_{max} of a process is often more complicated and degradation of gain per decade can be between 10-30dB depending on frequency range and transistor properties [11].

Finding out what is optimum NFmin for a given process is not as simple as looking at process datasheet for the f_T. NFmin optimization requires optimizing transistor dimensions and biasing. This was done using models of two process development kits (PDK) for CMOS: GLOBALFOUNDRIES 22FDX and 45RFSOI, and one PDK for SiGe BiCMOS: IHP SG13G2. For CMOS transistors, designer can adjust the length and width of the channel and also choose number of transistor fingers, making search space quite large. Respectively, the sizing of the SiGe HBTs and bias currents are two main deciding factor of gain and noise figure. Usually, it is only the number of emitter strips which can be varied to change the size of the transistor. The f_T and f_{max} of the three processes together with simulated NFmin and maximum stable gains for noise optimized transistors at 80GHz are shown in Table 1 [12]–[14]. Scaling of CMOS is clearly beneficial but due to different noise properties of HBT devices, the noise in SiGe is not as low as with similar speed CMOS process. NFmin for a transistor dimensioned for a typical LNA input stage is shown in Fig. 1 for SiGe and CMOS SOI technologies. NFmin values are estimated to be almost equal with the slight benefit for CMOS. They are referred to theoretical curves with respect to fT indicating also impact of extrinsic noise behavior. Calculated theoretical NFmin curves show that in order to reduce noise of a CMOS technology, the f_T has to be radically increased.

Predicting the impact of passives on the noise performance requires estimating the losses. Especially the losses of input matching components of the first LNA is critical to optimize as they have direct impact on noise figure. We studied models to find out minimum losses for capacitors for DC-blocks and

Table 1. Simulated minimum noise figures and maximum stable gains for for 130nm SiGe and 22nm and 45nm CMOS at 80GHz.

	22nm CMOS SOI	45nm CMOS SOI	130nm SiGe
f_T [GHz]	300	250	300
f_{max} [GHz]	450	250	500
NFmin [dB] @ 80GHz	2.51	2.72	3.1
Gmsg [dB] @ 80GHz	12.71	7.22	13.71

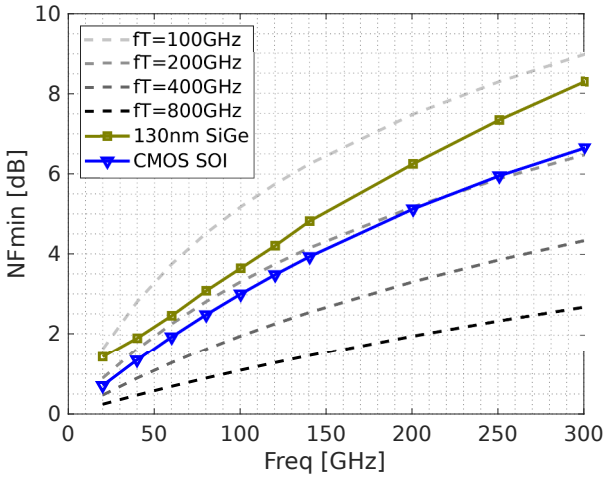

Fig. 1. Simulated NFmins compared to NFmin curves calculated from Lee's noise formula for different fT values.

for realistic frequency specific values. DC-blocks are used to isolate RF signals and DC-paths for example in preventing bias leaking to matching network. In LNAs a shunt inductor is often used for ESD protection purposes so a DC-block capacitor is often needed in the signal path. Our brief study concludes that all three processes are having high-quality RF capacitors providing less than 0.1 dB loss for typical RF capacitance values at 100GHz range.

For inductors, we compared processes with an inductor with same dimensions and lowest loss metal layer. Results of EM-simulated inductors are shown in Fig. 2. Aluminium layer used in SiGe process lower the Q for the inductor compared to higher conductivity copper inductors used in CMOS processes. Higher doping in 22nm compared to 45nm causes higher substrate losses which is seen in inductor Q.

Similar results have been reported from LNA designs at 28GHz from Rebeiz's group. Rebeiz's LNAs had similar inductances of 460-470pH, however, the Q-factors had drastic difference of 9 (22nm) and 28 (45nm) which in terms of power loss and noise figure increase is 0.49dB [15], [16].

III. Design Example LNAs

LNA design starts with the choice of topology which suits application the best. In this study, we aim for minimum noise in which common source/emitter amplifier is best. If noise can be traded-off with gain and bandwidth, cascode or common gate/base topologies could be used.

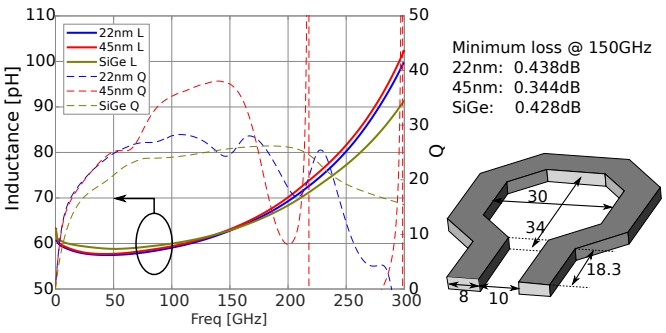

Fig. 2. Extracted inductances and quality factors of EM-simulations of inductors for 130nm SiGe and 22nm and 45nm CMOS. Dimensions in the illustration are in um.

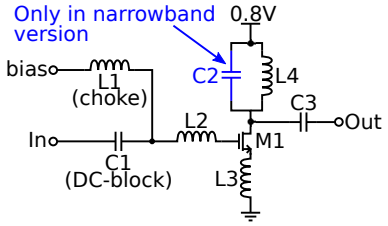

Fig. 3. Schematic used in LNA design exercise. Difference in narrow-and wideband LNAs is the load resonance strategy. In wideband version, resonance is formed with load inductor (L4) and transistor parasitic capacitances. Q of resonance is increased in narrowband version by adding a capacitor (C2) in parallel with load inductor since parasitic capacitances have lower Q than in capacitors.

RFIC design always is layout oriented and LNAs are not on exception. To design LNA from transistors with dimensions optimized for minimum noise figure, signal has to be routed to matching component level in the IC metal stack. Transistor device models are at lowest metal level which is part of digital routing metal layers, which are small in dimensions and in conductivity. Matching components are routed with higher metals to achieve higher Q-factors.

A set of LNAs were designed with 22nm library component models with progressive center frequencies starting from 50GHz. General schematic of LNA is shown in Fig. 3. Design was done in an iterative manner for input and output matching networks formed by L2 and L3 (input) and L4 and C2-3 (output) to achieve 50 ohm matching for input and output and minimum noise and maximum stable gain. Transistor size was increased from 10um used in Section II to 40um to get more power gain at small expense of noise. Then the transistor was routed to matching component metal layers whilst optimizing for minimum noise. Around 90GHz, the gain of a single LNA dropped to only 4dB and design was stopped. LNA loads were designed to have wideband and narrowband frequency response to which wideband proved to have better noise but at a cost of gain. Gain and noise characteristics of designed LNAs are presented in Fig. 4. Rapid degradation of gain is evident as the frequency is approaching a large fraction of process f_T/f_{max}.

Due to diminishing gain, more LNA stages are needed resulting in higher noise figure and power dissipation. The

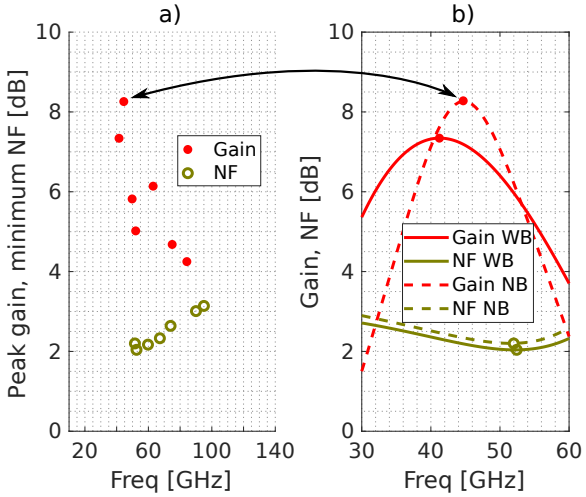

Fig. 4. Simulations of designed LNAs. Progression of peak gain and minimum noise figure with increasing center frequency is shown in a). Example of gain and noise figure curves for 50GHz wide (WB) and narrowband (NB) LNAs are shown in b).

impact of additional stages on noise figure was evaluated by cascading LNAs to reach a 20dB gain target and calculating resulting noise with Friis' formula. Fig. 5 shows three 20dB gain cascaded LNA noise figures compared against reported 22nm and 45nm CMOS LNAs and also against NFmin given by Lee's formula. Transistor f_T in this case is 230GHz at used bias point in which the simulated NFmin corresponds to Lee's formula with original constant of 2.3. Increasing the constant to 4 shows proposed theoretical minimum noise figure limit to reported works, effectively updating the formula constant to a practical implementation value which represents technology noise figure capabilities more closely. However, as noise becomes more and more gain limited, an exponential curve fit done on three exercise LNA points predict a diverging behaviour from Lee's noise formula after 70GHz or 30% of f_T. Measured noise figures back up this theory since two reported 140GHz LNA points are simulated and not measured. Whereas below 100GHz, the reported LNA noise figures also seem to follow an exponential curve but with more realistic implementation penalties compared to our design exercise with only library components.

Other reported CMOS, CMOS SOI and SiGe BJT LNA noise figures are shown in Fig. 6. For receivers below 100GHz, CMOS SOI is the best technology but likely due to higher gain, SiGe is currently dominating technology above 100GHz. The lowest noise curve represents fT of 300GHz with nominal noise multiplier (2.3) and the higher ones always 2x degradation between curves in noise behavior. The higher curves give good indication how complete LNAs compare against the input stage only performance.

IV. LNA and its Importance on Receivers towards 6G

Low noise amplifier is the most significant contributor for receiver noise in addition to lossy filter and switches between

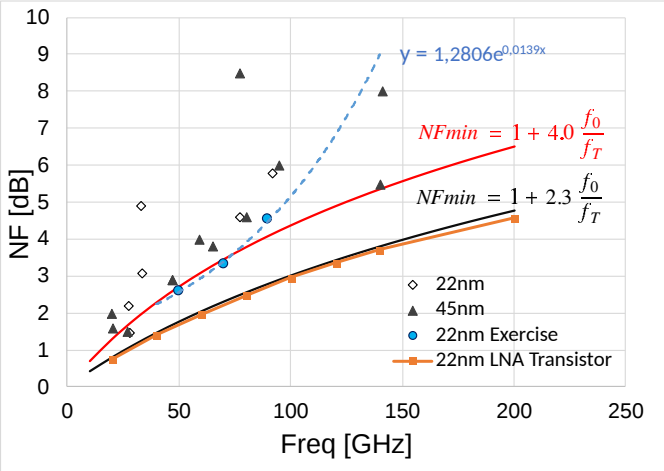

Fig. 5. Design exercise LNAs compared to reported works of 22nm and 45nm CMOS SOI LNAs with NFmin plots for 230GHz f_T.

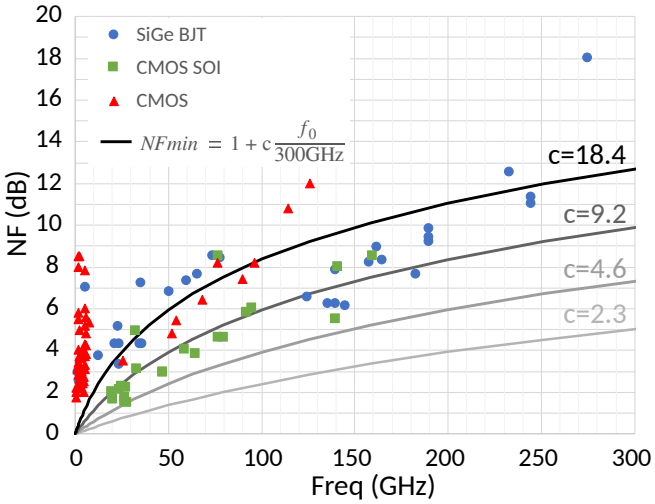

Fig. 6. Reported LNA noise figures for CMOS, CMOS SOI and SiGe BJT processes compared against calculated NFmin curves with different noise multiplier coefficients and 300GHz fT.

antenna and LNA. However, it is not the only contributor for the degraded noise figure if the LNA is not having sufficient gain. As described in the previous Section, loss of gain may become even more severe issue than noise in the RF front-end in system level at very high frequencies. This is illustrated in Fig. 7. Based on CMOS SOI data from our simulations and examples from the literature, a model on frequency scaling of gain and noise as a function of frequency was created. For one stage amplifier it is shown as gain1 and NF1. The shapes of the curves also represent the theoretical trend line from transistor physics and behavior depends on the transistor speed (f_T or f_{max}) as described above. Receiver noise analysis was done using (1) and the receiver total NF is plotted for one to four equivalent amplifier stages with mixer noise included. Mixer noise figure is shown as NFmix in the plot and it is based on a simple model that has equivalent shape but different factors than LNA model. Mixer noise is fundamentally higher than LNA with corresponding technology due to switching operation with the local oscillator but as a typical active mixer uses similar kind of voltage-to-current conversion transconductance at the input, one could assume corresponding noise scaling over frequency. Mixer can be understood here to include the rest of the receiver noise although in practical design there will be some smaller contributions also from subsequent amplifier and filter stages.

Dashed curves in Fig. 7 show total gain after one, two, three and four cascaded amplifier stages before the mixer. They describing the impact of net gain before mixer. Based on those, curves NFtot1-4 are calculated showing the total noise figure of the different scenarios. One can observe that the difference is small at low frequencies because a single stage LNA can provide sufficient gain to protect system from other noise sources. When gain drops and noise increases as a function of frequency noise of the subsequent stages becomes more prominent and the total noise figure starts to deviate rapidly from the best scenario i.e. single stage LNA. More stages are needed to keep the gain large enough. But even with four stages one can't reach the situation when noise of the mixer or rest of the receiver will become insignificant and impact of adding more LNA stages starts to disappear. Still these models predict that LNA can improve receiver noise figure as long as an amplifier stage can be designed to have some decibels of gain reducing the impact of the other parts. This has a lot of importance in link range and seems to have a contradiction of many mixer-first approaches published recently in circuit literature.

The study shows even with rather coarse and preliminary but circuit design based LNA model that the degradation of the receiver noise can not be predicted solely by using minimum noise figure of a single transistor or the first stage of the LNA. Even a typical multi-stage LNA will not provide sufficient net gain at frequencies approaching transistor speed limit. The situation will likely not improve much with new technologies either as intrinsic speed of a transistor is not easily achievable when interfaced with necessary passives at higher metal layers. The IC internal interface starts to impact the extrinsic speed achievable from the technology even without any package. Therefore this aspect needs to be taken thoroughly into account not only in antenna interface but specifically in radio system design when targeting to higher frequencies. Modelling constant noise over a large frequency range is simply not adequate. Also, this noise figure represents only the active part of the receiver consuming substantial amount of power per LNA stage and additional and often inevitable losses in the antenna interface will make the situation even worse. This should highlight the emphasis to find new approaches in antenna interface design with active electronics. In addition to that we have ignored here phased array aspects. If signal combining is done already at RF the array gain will protect us from mixer noise but on the other hand, RF phase shifter is typically more lossy and thus noisy than one LNA stage and loss of the combining network adds to that. Therefore the results can be considered also as the first guidance to RF

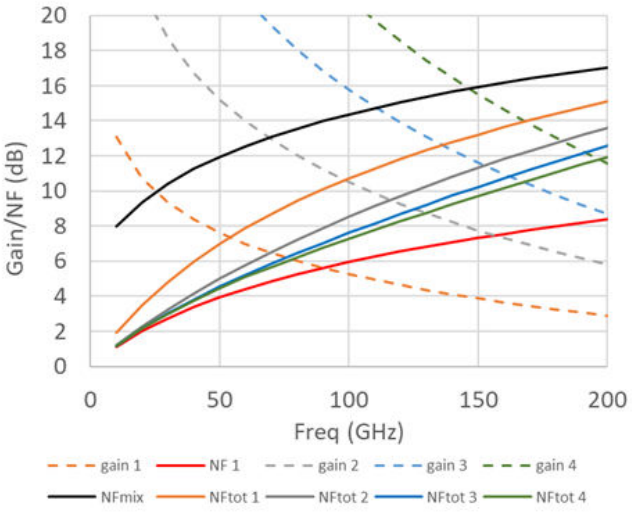

Fig. 7. Model of receiver noise and gain for one to four cascaded LNA stages with mixer.

beamformers.

V. Future Work

This work addresses the importance of the physical constraints coming from technology in RF and especially receiver design using the most critical component for noise i.e. LNA. The examples here are either from literature or from relatively simple design approach based on simulations. Both of these give guidance on the frequency scaling aspects towards higher data rates (i.e. higher carrier frequencies and bandwidths) but will not give comprehensive explanations to compare generally known trade-offs with realism in absolute scale. The literature examples are simply varying too much and designs using the same technology reference need to be done taking even many more constraints into account. That makes any IC design a unique solution to specific problem that and requires a complete implementation with experimental results to evaluate technology constraints more thoroughly in 6G context. However, the observations can be already utilized in current form for initial design of 6G radios when comparing the impacts of frequency scaling in relative scale to efficiently utilize the opportunities at different ranges of spectrum for different use scenarios. In the future, we will need both very thorough studies on practical technology and design constraints as well as new means to utilize them in 6G radio system design to optimize performance and system efficiency, like power consumption, the most optimal way. This is an aspect may be easily ignored both due to complexity and due to need for truly multi-disciplinary approach and interaction at the early phase of conceptual design.

VI. Conclusion

In this paper, we have explained physical facts and shown trends and challenges encounterd during the design of radio receivers for higher data rates and thus for higher carrier frequencies beyond 100 GHz towards 6G communications. Wireless link range does not only depend on the performance of antenna or capability of PA to generate power. It is also heavily dependent on the noise of the receiver that scales up with frequency where the output power of transmitter scales down in any semiconductor technology. In 6G considerations, we start to approach the technology limits of existing and also forthcoming silicon technologies and can't expect the same performance even from noise behavior that is often totally ignored in the system analysis. As silicon technologies may not perform well enough in the most data intensive scenarios in RF transceivers compared to other semiconductor technologies, which are not easy to integrate as a part of compact systems. However, they are needed to commercialize 6G with the goal of finding new circuit topologies and RF architecture concepts to overcome the challenge to continue with compact system. In last couple of decades, this approach was eventually the way forward in 5G mm-Wave solutions to achieve adequate performance. Hence, this is also one attractive research direction towards 6G.

This paper addresses the fundamental aspects of noise level increase from transistor theory and individual devices towards practical designs using simple LNA example scaled over frequencies. Performance is not only affected due to the degradation of noise parameter but also on reduced gain per stage as a function of frequency. Consequently, this leads to additional power consumption in the system. Principles of mapping the impacts to the whole receiver performance, such as range, sensitivity and other parameters, were addressed and projected results can be applied to receiver and radio link design for 6G system concepts for the perspective of local and as a part of heterogeneous network.

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