A 25 GHz Active Phase Shifter Using 10 bit Cartesian Control

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***Abstract*—This paper presents an active RF phase shifter, targeted towards 5G wireless systems, which uses an IQ vector modulator (IQVM) topology with a 10 bit cartesian codebook. The circuit is designed using 45 nm CMOS SOI technology. To generate the I and Q basis vectors for the IQVM, a tunable polyphase filter with a novel tuning mechanism is used, which allows operation over an octave of a frequency range, from 22 GHz to 40 GHz. The RF bandwidth of the proposed phase shifter is 2.5 GHz and can provide in excess of 8 dB of fine gain control over 360 degrees of phase shift. Active area occupied is 0.2 square millimeter. The total DC power consumed from 1 V supply is 36 mW.**

***Index Terms*—CMOS, IQVM, millimeter-wave, phase shifter, 5G.**

I. Introduction

Estimated data rates for 5G are almost 1000 times those of 4G. Furthermore, 5G should support extremely high traffic density [1]. To achieve this behemoth task, RF channels at millimeter-wave (mmWave) frequencies with higher bandwidth as well as phased array systems with beam steering capabilities are needed [2]. 3rd generation partnership project (3GPP) new radio (NR) FR2 standard has allocated several new mmWave frequency bands ranging from 24 GHz to 40 GHz, each having a bandwidth of 3 GHz [3]. Hence, in order to develop 5G compatible radios that can operate in 3GPP NR FR2 bands, wide band circuit blocks operating at mmWave frequencies are required.

In a phased array systems, the beam density is limited by the side lobe levels. In a uniformly spaced phased array, the theoretical minimum side lobe level is around 13.3 dB, provided that phase shifters with infinite phase and amplitude precision are used. Thus, in order to minimize out-of-beam interference while increasing the beam density, amplitude tapering is required. Amplitude tapering schemes such as Dolph-Chebyshev, Taylor, and Bayliss are proposed, of which Taylor being the most often used [4].

There are multiple ways to make a phase shifter, by vector summing orthogonal signals with different weights using a cartesian [5]–[7] or polar [8] codebook, and by changing the properties of a transmission line [9], [10]. The benefit of the vector summing method is its small implementation size but at the cost of power consumption. In this work, we chose the vector summing method in order to minimize the implementation size. The I and Q vectors are generated using a tunable polyphase filter (PPF). As the IQ vector modulator (IQVM) encodes both the phase and amplitude information in a single codebook, the number of bits dictate the available phase and amplitude resolution. This puts a limit on the amplitude tapering scheme that can be used. Thus, to determine the number of bits required in an IQVM, monte carlo simulations with random phase perturbation were done using Taylor amplitude tapering scheme. Weighing coefficients for two Taylor series were synthesized, one with a projected sidelobe reduction level of 20 dB (Taylor20) and another with 35 dB (Taylor35). As it can be seen from Fig. 1, with a 10 bit IQVM, Taylor20 series can achieve its target. Furthermore, for the Taylor35, the increase in sidelobe level rejection is marginal after ten bits. Hence, the IQVM is designed with a 10 bit control. GLOBALFOUNDRIES 45 nm CMOS SOI process is used for the design. Even though the core components of the phase shifter are designed to be either wide band or tunable, the RF bandwidth of the structure is limited to 2.5 GHz around a center frequency of 25.25 GHz. This limitation comes from the output driver stage.

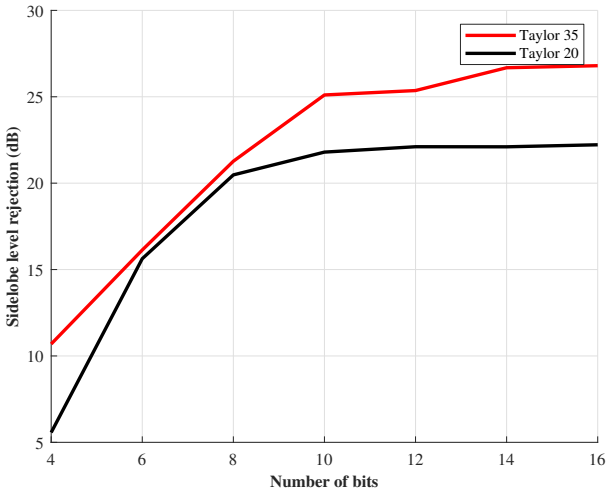

Fig. 1. Sidelobe level rejection as a function of number of control bits in the IQVM.

The organization of the paper is as follows, in Section II, the designed circuit is described, followed by the results in Section III. Conclusions are drawn in Section IV.

II. Circuit Design

The complete block diagram of the structure is shown in Fig. 2. The structure has a differential input and output

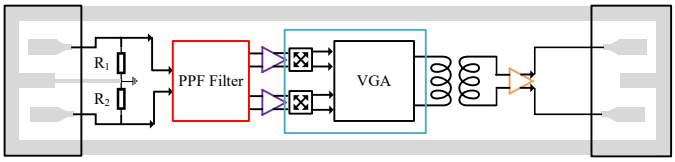

Fig. 2. Block diagram of the test structure with IQVM enclosed in the blue box.

and is designed to be tested using differential ground-signal-ground-signal-ground (GSGSG) probes. Resistors R_1 and R_2 are used for providing a wide band input matching. The first active stage is a PPF that is used to create the 90°I and Q base for the IQVM. The differential I and Q signals are amplified using differential amplifiers before IQVM. As the variable gain amplifiers (VGA) used in the IQVM are pseudo differential, true differential amplifiers are required to remove the common mode signal as the VGAs do not reject them. After IQVM the signal is applied to transformer based load. The secondary side of the transformer is connected to an output driver which is a narrow band differential amplifier, tuned to 25 GHz.

A. *Polyphase Filter*

The PPF is used to generate the 90°signal base that is required by the IQVM. Of the two different topologies of the PPF (constant phase difference and constant magnitude), a constant amplitude topology is used here in order to minimize the signal loss. Given that it is a single stage PPF, it can operate reliably only over a small frequency band around its center frequency. Thus, in order to have any tunability in the frequency of operation, either the resistors or the capacitors need to be tunable. In [5], variable capacitance was used and in [11], variable resistance was used. Here, variable resistors are used but the implementation is different compared to [11]. A fixed resistor along with different sized NMOS devices are used instead of a fixed NMOS with a variable bias as used in [11]. Furthermore, in order to provide higher linearity, bootstrapping resistors are used.

The schematic of the complete PPF can be seen from Fig. 3. Capacitors $C_{1\text{–}4}$ are a part of the main filter and are implemented using high Q vertical metal finger capacitors. Resistor R_1 is sized so that the PPF operates at the lowest frequency. The NMOS are sized so that when all of them are in the ON state, the effective resistance moves the PPF operating frequency to the maximum. Capacitors $C_{5\text{–}10}$ are for AC coupling. The simulated performance of the PPF is shown in Fig. 4. Here, the red curve corresponds to the frequency at which the generated I and Q vectors have exactly a 90°phase shift, and the blue curve represents the amplitude mismatch between the differential I and Q vectors at that frequency.

B. *Differential Amplifier*

In order to cancel the common mode signal of the PPF, a true differential amplifier is needed. Furthermore, the gain provided by the differential amplifier is approximately equal to the attenuation caused by the PPF, thus maintaining a

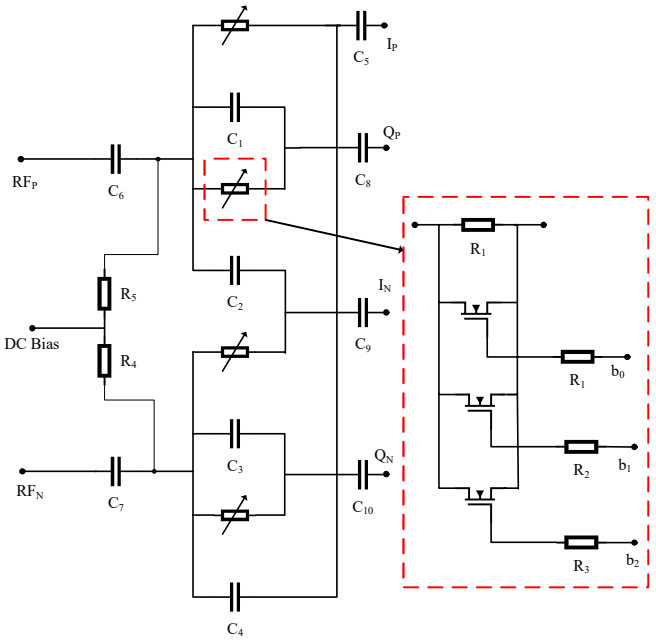

Fig. 3. Schematic of the PPF.

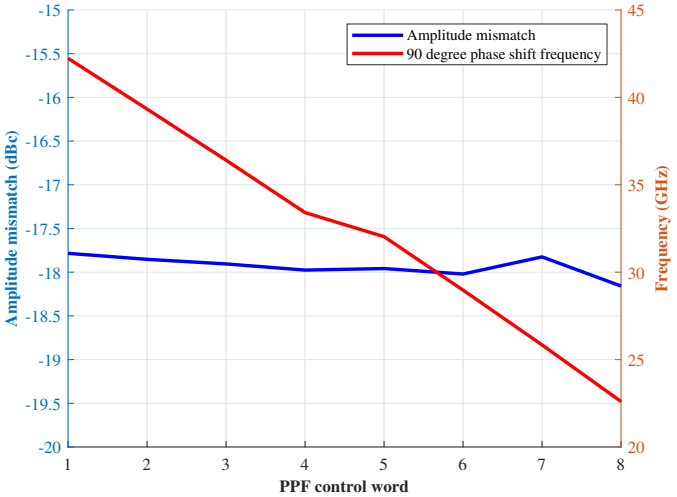

Fig. 4. Amplitude mismatch and 90°phase shift frequency the PPF as a function of its resonance control word.

constant signal level. The schematic can be seen from Fig. 5. To have a small tunability in the gain, instead of having a fixed load, a variable load in the form of a DC biased PMOS is used. Transistors $Q_{1\text{–}2}$ have a width of 24 µm. Given that the common mode rejection ratio (CMRR) of the amplifier will be governed by the impedance seen at the source of Q_1 and Q_2, an inductor L_1 instead of a tail transistor, is used. The reasoning for that is related to the large c_{ds} of the tail transistor, which drastically degrades the high frequency impedance seen by the common mode signal, thus reducing the CMRR.

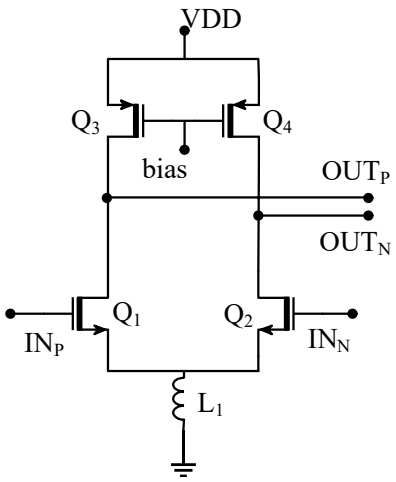

Fig. 5. Schematic of the differential amplifier used after the PPF.

C. IQ Vector Modulator

At block level, the IQVM consists of two distinct blocks as can be seen from Fig. 6. The first is for selecting the polarity of the basis vector, which is followed by pseudo differential trees. Cross connected PMOS are used for switching the polarity of the signal. As there are two polarity selectors, one for I and one for Q, two out of total ten bits are used for polarity selection.

After the polarity selection, there are eight binary weighted trees, four for I and four for Q branch. The schematic of one of the trees can be seen in the lower right half of Fig. 6. From each of those four, two of the RF trees are fed with the input RF signal and they contribute RF signal towards the output. The other two dummy trees are just biased and not driven by the RF signal. Their controls are chosen complementary to to the active trees, and their main purpose is to keep the output capacitance of the total IQVM constant independent of the control word. The main purpose of having the dummy trees is to keep the capacitive loading, as seen by the inductive IQVM load, at a constant level irrespective of the control value.

III. Results

The structure is designed and sent for fabrication using $45\,\mathrm{nm}$ CMOS SOI technology. Hence, only simulated results are presented. The complete layout of the structure is shown in Fig. 7. The dimensions including the input and output pads is $0.454\,\mathrm{mm} \times 0.888\,\mathrm{mm}$. The core area is $0.2\,\mathrm{mm}^2$ and is enclosed by a green rectangle in Fig. 7. The maximum DC power consumed from $1\,\mathrm{V}$ supply by the phase shifter is $36\,\mathrm{mW}$.

Simulated differential S-parameters are shown in Fig. 8. As the input matching is achieved using resistors, it is broadband and does not vary much as a function of frequency. The output of the phase shifter is tuned for $25.25\,\mathrm{GHz}$, as can be seen from the S21 curve. The structure has a RF 3 dB bandwidth of $2.5\,\mathrm{GHz}$, with $24\,\mathrm{GHz}$ and $26.5\,\mathrm{GHz}$ being $-3\,\mathrm{dB}$ corner frequencies. Simulated large signal response can be seen from Fig. 9. The input 1dB compression point is around $3\,\mathrm{dBm}$.

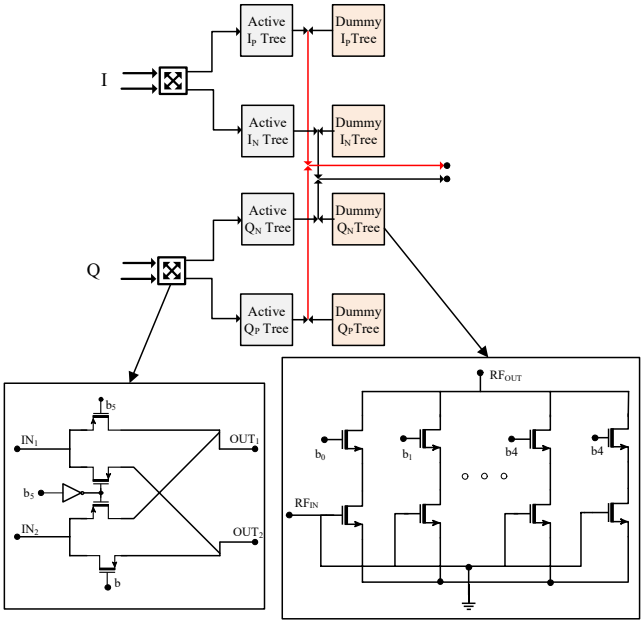

Fig. 6. Block diagram and schematic of the IQVM.

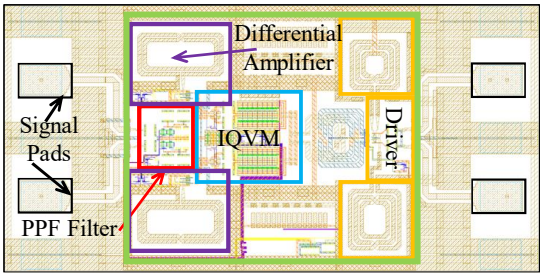

Fig. 7. Complete layout of the test structure.

All 1024 different phase and amplitude points, simulated at $25.7\,\mathrm{GHz}$, are shown in Fig. 10. The color of the points is used to encode the power, with the red color points having highest power, green color points having $2\,\mathrm{dB}$ less than that and so on. The red color points, which are only situated on the four edges, have a coarse phase resolution over complete $360°$. This is due to the cartesian nature of the IQVM. All the other color bands show a more precise control over the complete $360°$range and also provide a fine gain control of not less than $8\,\mathrm{dB}$.

The small signal noise spectrum can be seen from Fig. 11. The integrated small signal noise from $24.5\,\mathrm{GHz}$ to $26.5\,\mathrm{GHz}$ is $459\,\mu\mathrm{V}$. This has been simulated with the IQVM at its highest power setting.

IV. Conclusion

In this work, we demonstrated an active phase shifter IC targeted toward 5G communication systems. The proposed mmWave phase shifter has a RF bandwidth of $2.5\,\mathrm{GHz}$ and a center frequency of $25\,\mathrm{GHz}$. The design includes a novel single stage tunable PPF which gives it an operating range of

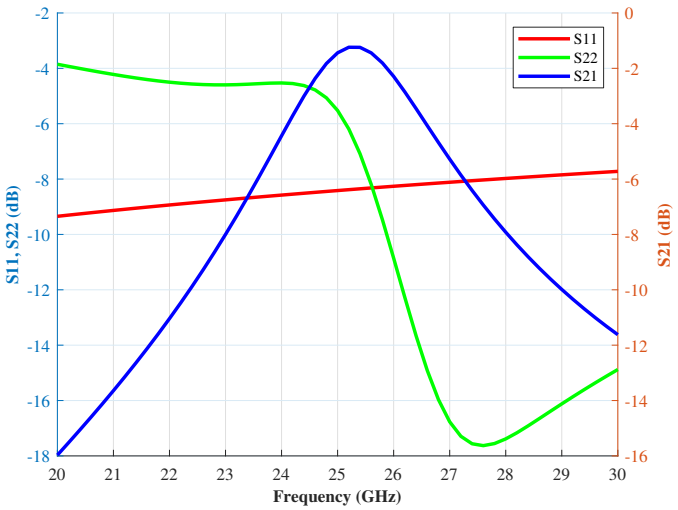

Fig. 8. Simulated differential S-parameters.

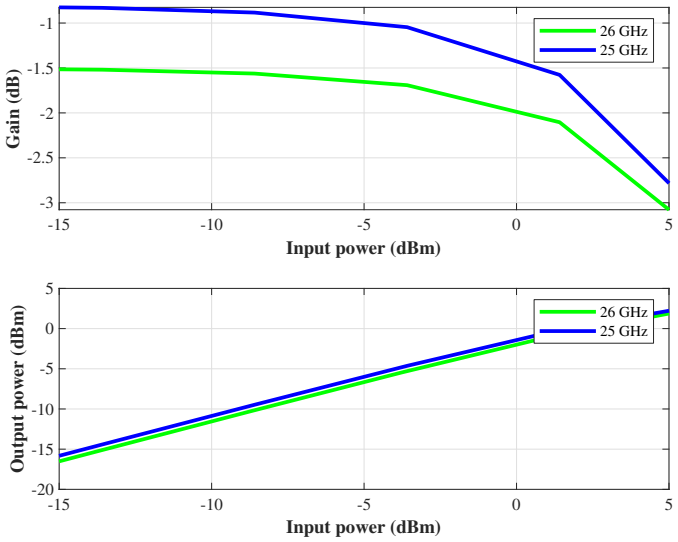

Fig. 9. Gain and output power as a function of input power.

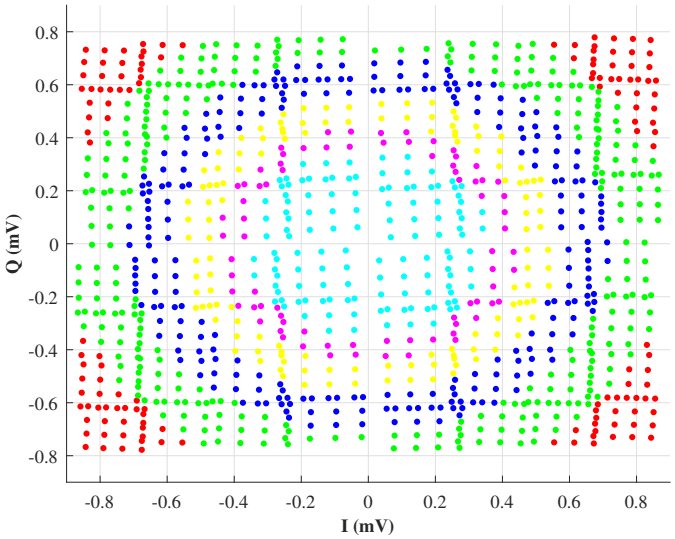

Fig. 10. Gain and phase points at 25.7 GHz.

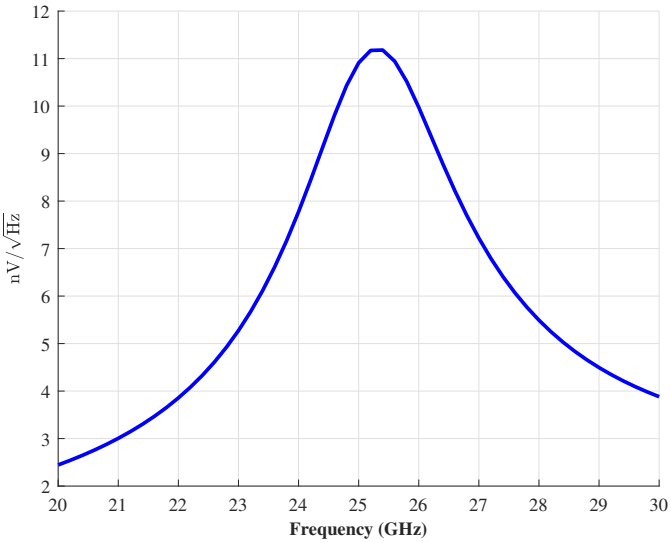

Fig. 11. Small signal noise spectrum.

over an octave. The core internal blocks of the phase shifter (PPF, differential amplifiers and IQVM) were designed to operate from 22 GHz to 40 GHz and only its output driver limits the RF response. The DC power consumed while operating from 1 V was 36 mW. The structure can provide in excess of 8 dB of fine gain control along with precise phase control over the complete 360°range. The integrated small signal noise at the output over the RF bandwidth was 459 µV.

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