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Non-Destructive Characterization of Glass Laminated Electronics

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***Abstract*—By integrating electronics inside the laminated glass, the windows and structural glass elements can be transformed to be functional and interactive. Once the electronics is embedded into the glass in lamination process, the electronics is exposed to different type of stresses, having an influence on performance and reliability. In order to understand the consequences of lamination and to explain the reason for failures, non-destructive optical coherence tomography (OCT) based method was used in this study. In addition, thermo-mechanical simulations were done to find possible causes for observed failures in light emitting device (LED) chips and wirings. Combining the analyzed OCT data with simulations, was shown to be very effective tool to select right materials and optimize the lamination process for glass embedded electronics.**

Keywords—printed electronics, hybrid electronics, optical coherence tomography, simulations

I. INTRODUCTION

Glass is one of the most widely used material in architectural designs, enhancing the interiors and exteriors of the buildings [1]. Another main application field for glass is in automotive industry where laminated glass is used in windshields of the vehicles [2]. Laminated glass structures are widely used in both architectural and automotive glasses due to their excellent properties. Recently, different kind of functional elements are embedded inside the glass laminate to make transparent functional structures with controllable features and Internet of Things (IoT) connectivity, highly appreciated in modern urban spaces.

Integration of electronics in the laminated glass is based on the latest knowhow of materials and manufacturing technologies. In this new approach, functional components are not just covered by glass, but it is embedded as solid part of the glass laminate, making it different from the conventionally used glass protected devices. Due to the relatively low maturity level of the technology, the lack of knowledge about the optimal materials and manufacturing parameters, quality, products' life time and performance prevents the implementation of data based products and service enabled by this technology. In addition, a high yield mass manufacturing processes for these products is still under development. In order to find reasons for failures caused by the lamination and find ways to optimize the manufacturing process, novel non-destructive testing methods for characterizing are needed. That is why the optical coherence tomography technology (OCT) measurements with complementary thermomechanical simulations are carried out in this study.

OCT is an optical measurement technique mostly used in medical applications [3] but past few years same technology has been used in industrial applications such as material research [4], material interaction measurement [5], rheology [6-7], wettability [8], electronics testing [9,11], etc. However, according to our knowledge, OCT investigation of glass laminated electronics has not reported before. In addition, the simulation based analysis of observed OCT findings is also completely new aspect. This paper is focused on evaluation of the effect of lamination process to the light emitting diodes (LED) on carrier plastic foil.

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II. MATERIALS AND METHODS

A. Glass Laminated LED foil

Measured and simulated glass laminate structure consists of PET carrier foil with screen printed silver wiring needed for powering and controlling the 16 pcs of LED chips glued with conductive glue on the contact areas and support glue on the edges of the chip. Silica glasses and polyvinyl butyral (PVB) based intermediate layer were used as glass laminate. The schematic of measured laminate structure is shown in Fig. 1. More detailed description of the used materials and components are described in Table I.

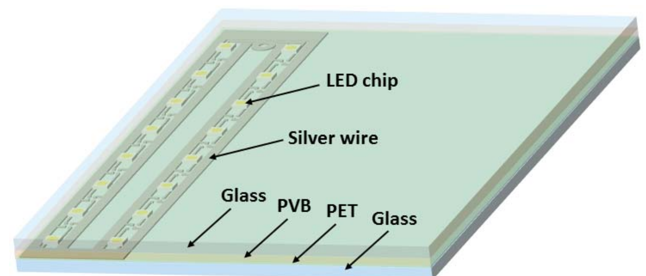

Fig. 1. Schematic illustration of measured glass laminated with LED chips and screen printed wiring (not in scale).

B. Optical Coherence Tomogaphy

Non-destructive characterization of laminated electronics structures were done with the commercially available OCT device (Hyperion, Thorlabs Inc.). The axial (depth) and the lateral resolution of the system are 5.8 (in air) μm and 8 μm respectively. Tomographic images of laminate are acquired by raster scanning a probing beam over the sample. The probing beam was aligned in a small angle in relation to the glass laminate surface to reduce the strong backscattering from surface to improve the sensitivity of the measurements inside the laminate.

TABLE I. PARAMETERS OF THE MATERIALS USED IN SIMULATIONS

Component	Material	Coefficient of thermal expansion [1/K]	Heat capacity at constant pressure [J/(kg*K)]	Density [kg/m^3]	Thermal conductivity [W/(m*K)]	Young's modulus [Pa]	Poisson's ration
Glass	Silica glass	5.50e-07	703	2203	1.38	7.31E+10	0.17
PET-film	Polyethylene terephthalate	3.9e-5	1300	1430	function (215-325K)	function (77-300K)	0.43
Lamination layer	PVB	170e-6	1980	1066	0.2	20000000	0.45
Led chip package	Nylon 66	95e-6	1700	1140	0.28	1.7e9	0.4
Led encapsulant	Silicone	function (293-443K)	function (225-300K)	function (293-443K)	function (250-300K)	function (293-443)	function (293-443)
Support glue	Acrylic	97e-6 (293- 323K) 215e-6 (323-450K)	1500	1080	0.2	175000000	0.37
Wiring	Silver	function (30-300K)	function (75-1235K)	function (140-873K)	function (250-1235K)	function (0-1173K)	function (0-1173K)
Contact paste	Ag filled epoxy (85 wt% Ag)	26e-6 (293-353K), 93e-6 (353-473K)	787	3070	function (293-403K)	4.4 e9	0.33

C. *Thermo-mechanical simulations*

The COMSOL Multiphysics 5.3. software was used in the simulations. The heat transfer module and structural mechanics module was used for thermal conduction modelling and thermal expansion and stress simulation, respectively. Multifrontal massively parallel sparse direct solver was used in time-dependent simulations. The area of the model is 17 mm by 17 mm, covering only one LED chip with wiring (Fig. 2). The applied model has large range of size features (from μm to mm) and they were dynamically meshed in order to keeping the simulation time and memory requirements reasonable. Constructed 3D-model consists of LED, and conductors on polyethylene terephthalate (PET) foil, which are laminated between two glass sheets with PVB interlayer. The 3D-model consist of eight sub-components, which each are from different materials (see Table 1).

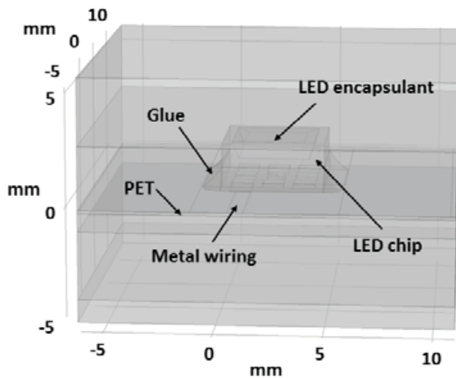

Fig. 2. 3D simulation model of the LED chip (with package) on PET foil with silver wiring laminated inside the glass with PVB.

The parameters for silicone and silver could be found from the COMSOL libraries but the other materials were lacking of some or all of the parameters. For those, the missing parameters were estimated from data found in data sheets of those materials. The exact material composition a LED chip and support glue, were not known. These values were estimated from datasheets of corresponding materials. For example, in the case of LED chip, parameters were obtained from Nylon 66 for which data was available. All the used material parameters are summarized in Table 1.

Many of the parameters were defined as the functions of temperature (obtained from COMSOL libraries). In some of the cases, the simulated temperature is higher than the defined range of the function. In such cases the parameter values are extrapolated as a constant, and the last known value of the function is used.

The 3D-model is heated at a constant temperature to simulate a thermal conduction during the lamination. The simulated temperatures are used to estimate a thermal expansion and resulting stresses inside the components. In the simulation of thermal expansion, a bottom boundary of the model is fixed. For the temperature, the top and bottom boundaries are set to 165°C (438.15K). The total heating time of the component is set to 100 s.

III. RESULTS

This section is divided into two main sections. The first describes the results of thermomechanical simulations and the second the findings of conducted OCT experiments.

A. *Simulations of lamination process and analysis*

The simulations have done to analyze the thermomechanical stresses caused by the lamination process. After removing the gases from the laminate by vacuum, laminate is heating to bond glasses firmly together.

Within the first 5 seconds of heating, the temperature in the glass-PVB interface has risen over 80 °C. Once the laminate heating is continued 20 seconds, the LED chip is heated around 100 °C (Fig. 3). After 50 s, the temperature of the LED chip is already over 160 °C (Fig. 4). Worth to notice that, the color bars in the Fig. 3. and 4. are have different ranges. Since the metallic wiring has high thermal conductivity (≈8 W/m*K), the fast heat transfer can be seen as decreased temperature elevation at the contact points.

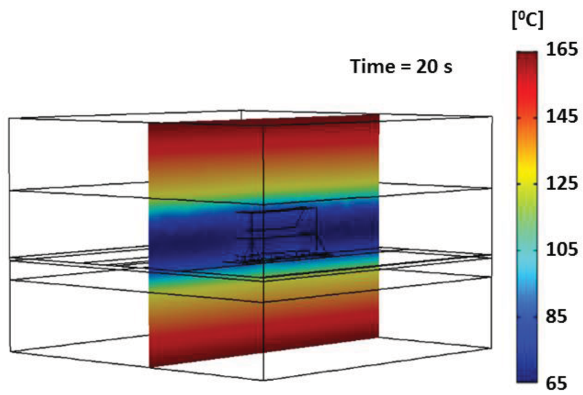

Fig. 3. Thermal conduction in the glass laminate after 20 s.

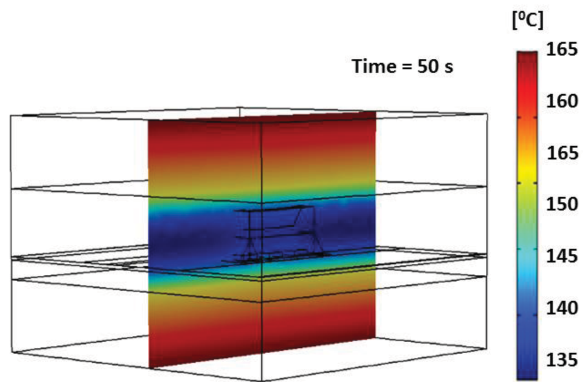

Fig. 4. Thermal conduction in the glass laminate after 50 s.

Temperatures obtained from the heat conduction were utilized in calculation of time dependent thermal expansion of the materials. Thermal expansion in the lateral direction (y-axis) at 50 sec. is depicted in Fig. 5. In this Fig., the origin of y-axis is in the center of the LED chip (middle of the image). Especially the PVB is clearly seen to expand during the heat treatment, causing some extruding of the PVB on the edge of the laminate.

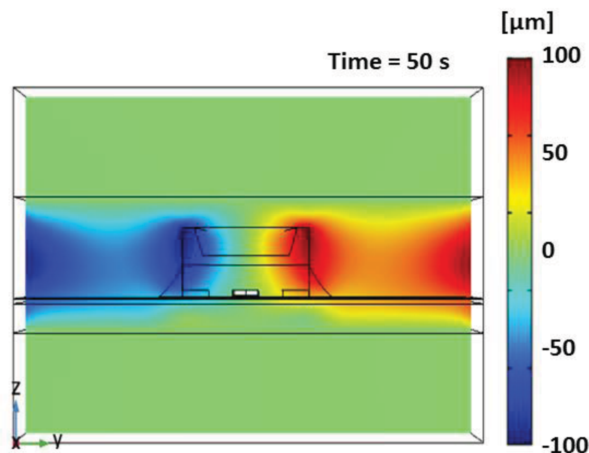

Fig.5. Thermal expansion in lateral direction (y-axis) at 50s.

Since the thermal expansion coefficients of the used materials are different, thermally induced stresses are seen in the laminate. To quantify the stress, so called Von Misses stresses are calculated. In Fig. 6, the origin of high stress values are seen already after 5 second of heating in the interface of conductive wires and the LED chip.

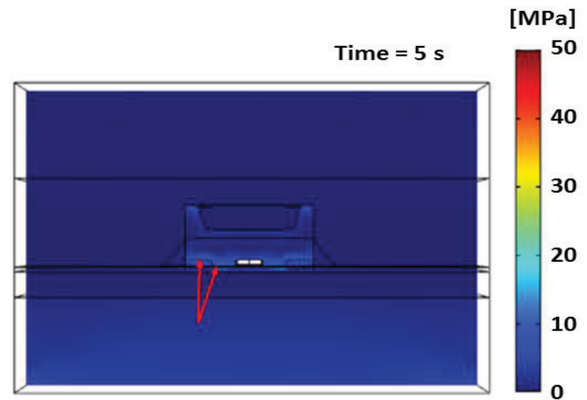

Fig.6. Von Misses stress distribution inside the laminate at 5 s. The highest stress consentration points are seen on the interface between LED chip and conductive silver wire (red arrows).

As the temperature is elevated inside the LED chip, the high stress appear also inside the PET foil. These locations are on the edge of support glue (Fig. 7.). Von Misses stress is increased on the interface of the LED chip and encapsulant.

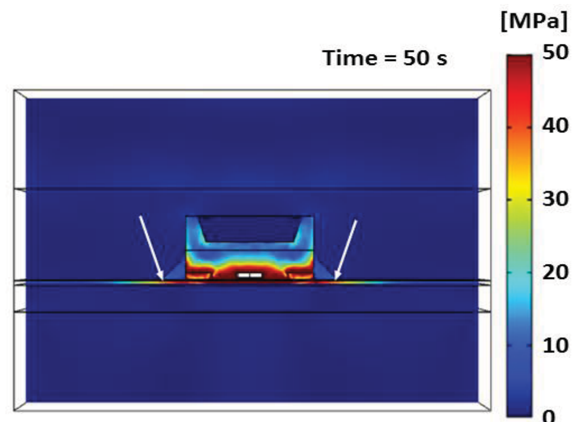

Fig.7. Von Misses stress distribution inside the laminate at 50 s. The high stress concentration points are seen on the interface between PET and supporting glue (white arrows).

B. OCT measurement results and analysis

Based on the above described simulations, the high stresses are concentrated on specific locations. Connection point of the supportive glue and PET was expected to be a potential location for failures. Another high stress areas were in the proximity of LED chip and conductive wires. Even though, OCT is capable for rather fast measurements, the sample were visually inspected before actual measurements to find interesting features and for further investigation. That is reducing the need for excessive data acquisition and processing.

The OCT measurements were performed from the both sides of the sample to get the best possible images of structures in the proximity of PET around the LED chip. The measured area covers the junction of glue-PET and the chip-wire junctions. A location close to chip with possible defect were measured. Obtained results are shown in Fig. 8.

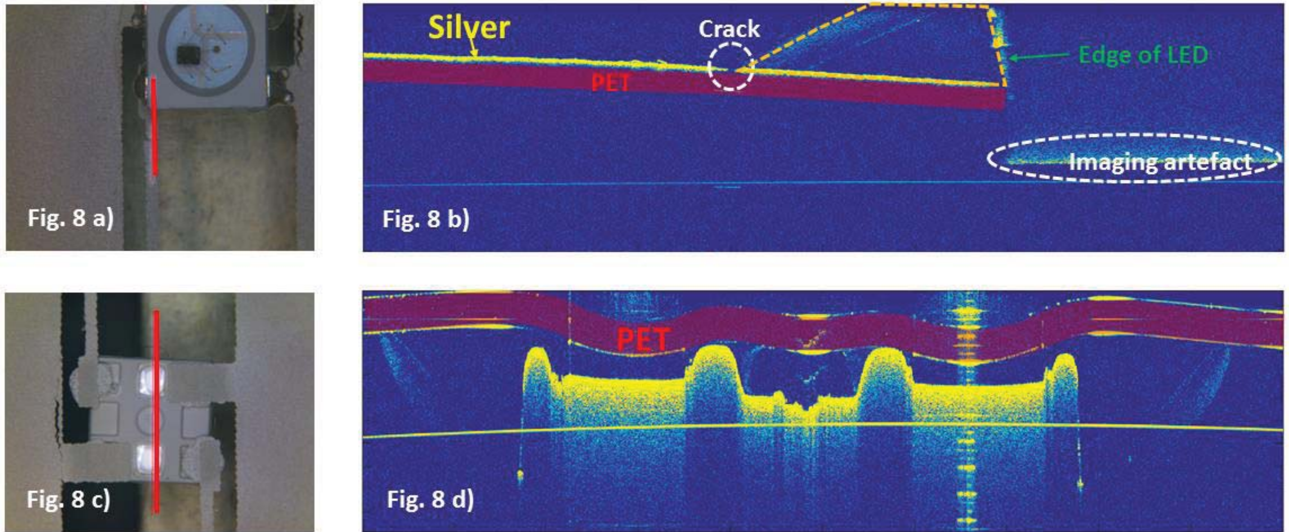

Fig. 8. OCT cross-sectional images of laminated LED chip. 8a) Photography of the measured area (red line indicates the location for the OCT cross-section image); 8b) OCT cross-sectional image from upper side of the glass laminate; 8c) Photography of the measured area (red line indicates the location for the OCT cross-section image); 8d) OCT cross-sectional image from bottom side of the glass laminate; Some key features are marked to 8b) and 8d) to make image analysis more intuitive.

In the Fig. 8b) the intensity of the OCT signal is reduced significantly on the junction of conductive wire and supportive glue. That is clear indication of the breakage of the metallic wire, because the light is not highly backscattered from that location. It is worth to mention, that high stress were simulated to be exactly in the same location. The imaging artefact underneath the LED chip in Fig. 8b) is caused by the high reflection of the upper surface of the LED chip (which is not visible in the Fig.).

The bending of PET underneath the LED chip is clearly seen in Fig. 8d). Due to the fact that pins of the LED chip are much harder than the other materials in near proximity of the interface, PET bends due to the stresses during the lamination. Based on the simulation, temperature gets higher than the glass transition temperature of PET during the lamination. Once the plastic is over that temperature, its structure is easily deformable. However, the origin for the PET bending cannot be explicitly explained by the simulations or the measurements.

Since the LED chips are glued on the PET, there is expected to be gas underneath the chip sealed by the supportive glue. In the Fig. 8d) some additional layers are seen beneath the chip. Those layers are expected to be trapped gas. However, that observation is difficult to be confirmed without destroying the sample.

In both Figs. 8b) and 8d), additional layer between the supportive glue and PVB are observed. The origin for this layer is not known.

C. OCT measurement of non-laminated LED chips on PET

To avoid high reflections and artefacts cause by glass laminate, the sample without glass laminates were also measured. Sample with LED chips glued on PET was heated and cooled (up to 85 degrees of Celsius) to cause thermomechanical stresses to the structure comparable with the temperatures caused by the lamination heat treatment.

LED chip were imaged by OCT from upper side and the obtained results are shown in Fig. 9. It can be clearly seen that encapsulant is detached from the LED package caused by the thermal expansion stress correlating with simulations. It seems that bonding wire was also cut by the forces causing failure of LED. Detailed analysis confirmed that part of the encapsulant is splitted during the detachment. Detailed OCT image used as a basis of that analysis is shown in Fig. 10.

IV. Discussions and conculsions

High stress concentration points estimated by thermomechanical simulations supports well the observed failures and defects measured by OCT such as the breakage of conductive wires on the edge of supportive glue (Fig. 8b). Similar kind of correlation were found in case of chip encapsulant detachments (Fig. 9b). Some of the most prominent cracks and detachments were able to be

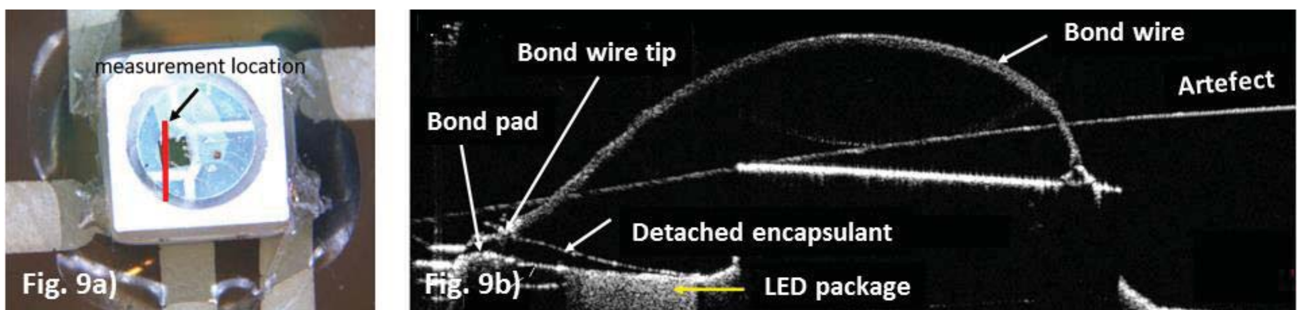

Fig. 9. OCT cross-sectional images of laminated LED chip. 9a) Photography of the measured area (red line indicates the location for the OCT cross-section image); 9b) OCT cross-sectional image from upper side of the glass laminate.

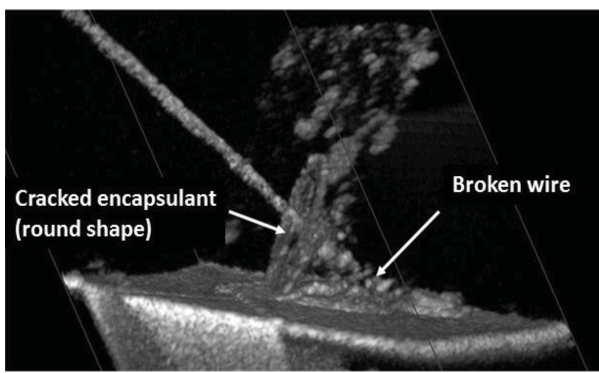

Fig.10. OCT volume rendering image of cracked LED encapsulant.

distinguished by visual inspection, confirming the observations and analysis made by OCT. It is worth to notice that in the case of non-laminated LED chip, the thermo-mechanical stresses are distributed slightly differently than in laminated structure.

The unknown interface between the supportive glue and the PVB interlayer were observed by OCT (Fig. 8b). That interface is slightly scattering indicating some porosity or chemical inhomogeneity of the layer. The thickness of that layer is around 200 μm measured by OCT. The performed simulations indicated that the origin for that layer is unlikely explained only by the thermal expansion. Thermal expansion might have a role on it but some other phenomena is having an influence on that. Spectroscopic analysis of the layer or non-destructive chemical analysis of the structure could provide more information about the layer. This unknown layer might negatively influence on the reliability of the electronics laminated in glass and due to it scattering characteristics, some unwanted optical distortions or reflections are expected once LEDs are turned on.

The simulation model has some limitations such as some of the material parameters are not precisely know and some of the structural features of the LED chip for example, has not taken into account during the simulation. Despite the limitations of current version of the model, the simulation results provides valuable information about the origins of the failures caused by the lamination process. Detailed understanding of the failure mechanisms provides crucial information for selecting the right materials and design structures to be used in this type of applications. However, further development of the model and verifications are needed.

The combination of simulations with comprehensive OCT imaging is very interesting approach for non-destructive testing of different type of materials and structures. Proposed approach is especially interesting for industrial applications but can be applied in biomedical field as well (where the OCT is widely used).

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