Ka-Band Stacked Power Amplifier on 22 nm CMOS FDSOI Technology Utilizing Back-Gate Bias for Linearity Improvement

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***Abstract*—This paper presents a method for extending millimeter wave power amplifier (PA) linear range by fine tuning the CMOS SOI device output characteristics via back-gate biasing. The effect of back-gate biasing to PA performance is measured and reported. It is demonstrated how implementing the same bias point with different back-gate values affects the linear range of the fabricated PA. By applying positive back-bias to the NFET devices, the measured PA displays minimum AM-PM and reaches maximum output power, PAE and $1\,\mathrm{dB}$ compression point of $16.3\,\mathrm{dBm}$, $23\,\%$ and $13.9\,\mathrm{dBm}$, respectively. EVM of $6.8\,\%$ and ACLR of $-29.3\,\mathrm{dBC}$ were achieved at $5\,\mathrm{dBm}$ average output channel power with a $100\,\mathrm{MHz}$ 64-QAM OFDM signal.**

Keywords—power amplifier, PA, CMOS, SOI, back-gate, mmWave, 5G.

I. Introduction

It has been suggested that 5G millimeter wave transmitters employ large phased arrays to achieve beam steering capability and the required effective isotropic radiated power (EIRP) [1]. At the same time millimeter wave (mmWave) applications are aimed for high data rate applications, which leads to use of modulation schemes of high peak to average power ratios. This means that potentially hundreds of low power integrated front end PAs in parallel must be used in deep back-off, typically with poor efficiency. This leads to impractical battery life in mobile devices and, due to cooling, increased size and material costs in the base station side.

In this paper we describe a fully integrated three-stack power amplifier (PA) at Ka-band using GLOBALFOUNDRIES 22 nm CMOS fully depleted silicon on insulator (FDSOI) technology [2]. It will be shown that by utilizing back-gate bias it is possible to affect the linearity and available output power of the proposed PA.

The organization of the paper is as follows: Section II presents the PA design and the use of back gate biasing on it, Section III shows the experimental results and conclusions are drawn in Section IV.

II. Back-Gate Enabled Stacked Power Amplifier

The PA in this work was implemented with GLOBALFOUNDRIES $22\,\mathrm{nm}$ CMOS FDSOI technology. A major benefit of the SOI technology for PA design is the possibility to increase the VDD by stacking the transistors and so enhance the achievable voltage swing at the output stage [3]. With buried oxide separating the diffusion regions from the substrate, the large output voltage can be divided among the stack by connecting the transistors in series, without causing source or drain to substrate breakdown at any stage. For the same reason the transistors can handle large body (back-gate) bias without any current leakage to the substrate.

Back-gate effectively offers a fourth terminal to control the FET. In [4] back-gates of a three-stack PA were set to same value as VDD, but the impact was not further evaluated. It was reported in [5] that increasing positive back-gate bias of a NFET device with fixed gate bias improves f_T and hence could improve linearity. However, if gate voltage is kept constant and back-gate tuned, operating point, in terms of drain quiescent current, is going to change. Based on simulations, f_T change is negligible if the quiescent current is kept constant by lowering gate voltage while increasing back-gate voltage. In this paper we examine how setting the same bias point with couple of different gate and back-gate combinations affects the operation.

The starting point of our analysis is a single NFET transistor in common source configuration. Fig. 1 shows the simulated transconductance behaviour. It can be seen that applying positive back-bias increases the maximum achievable drain current value for the given V_{gs}. At the same time threshold voltage reduces and the transistor turns on and saturates earlier. The threshold voltage adjustment ratio to the applied back-gate voltage is approximately $80\,\mathrm{mV/V}$. Another route for trying to equalize the currents would be to scale down V_{ds} for increased V_{bg}, but in order to maximize the voltage swing at the output the first approach is preferred.

Simulated output characteristics are plotted in Fig. 2. Results indicate that even if increased back-gate bias is compensated by lowering the gate bias by $80\,\mathrm{mV/V}$, the transistor can draw more current with a given V_{ds} with high V_{gs} values. With lower gate overdrive the output remains approximately the same. Simulations reveal also that with positive back-gate bias the device displays slightly degenerated g_m value in subthreshold region, but ends up achieving greater g_m in saturation. This may be due to subtle changes in subthreshold slope behaviour, which in turn is sensitive to bulk-channel depletion capacitance [6].

A. Three-Stack Ka-band Power Amplifier

The schematic of the demonstrated PA is shown in Fig. 3. The PA consists of a stack of three transistors with separate bias enabled for each gate and back-gate. Gate impedances are optimized so that the voltage swing is divided across the

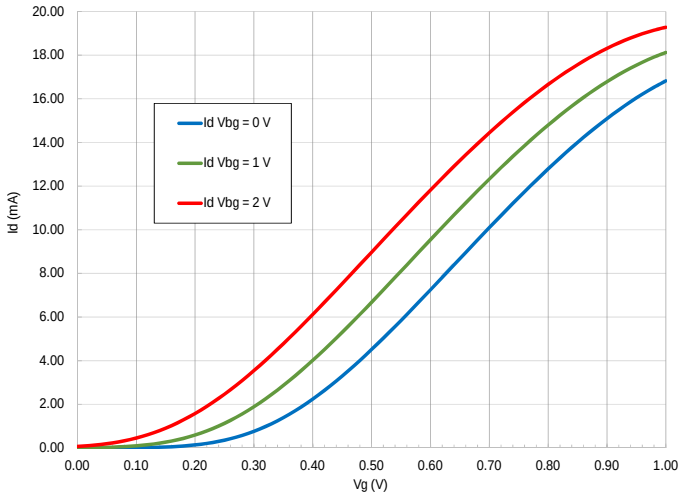

Fig. 1: Transconductance characteristics with multiple back-gate values and V_{ds} = 800 mV.

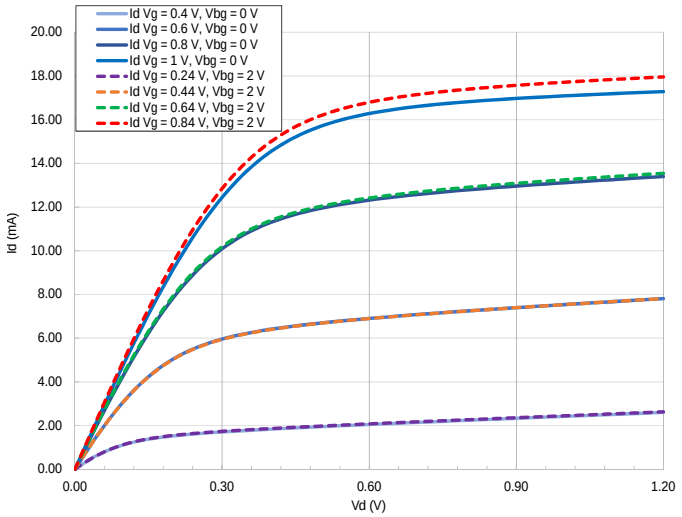

Fig. 2: Output characteristics with two back-gate values.

stack. Back-gates are biased through high value resistors in order to minimize parasitic drain to bulk and source to bulk capacitances. Stacking three transistors enables 2.8 V VDD. The gate impedances of the transistors are optimized for the inter-stage matching and voltage swing in the source nodes of M2 and M3. Keeping the source waveforms synchronous and progressively increasing is essential in terms of avoiding breakdown. The magnitude of the gate capacitances required decreases as one moves up in the stack i.e, C2 is bigger than C3. Input and output are both transformer matched. The transformers serve also as DC blocks.

III. Experimental Results

A. Measurement Setup

The micrograph of the PA along with the single tone measurement setup is shown in Fig. 4. The layout dimensions with pads are $629\,\mu\text{m} \times 337\,\mu\text{m} = 0.21\,\text{mm}^2$ and the active area is $0.07\,\text{mm}^2$.

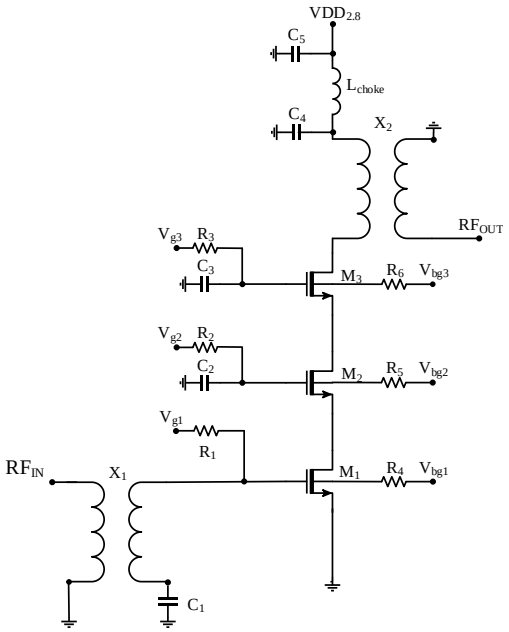

Fig. 3: Circuit diagram.

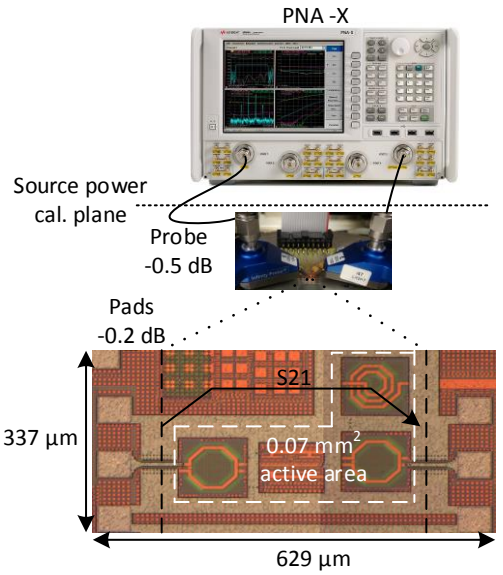

Fig. 4: Single tone measurement setup and chip photograph of the fabricated PA.

S-parameters measurements were conducted using Keysight PNA-X network analyzer and Cascade Infinity I40 probes. S-parameter measurement reference plane was calibrated to the probe tips using Cascade calibration substrate P/N 101-190, meaning that the measurement results include pads.

In single tone measurements, the source power was calibrated to the end of the input cable and the S21 measurement was normalized using on-chip Thru standard. Pad and probe losses were measured and taken into account in the shown results. The input power was swept and the PA metrics could be determined with the knowledge of the measured S21

and corrected input power.

Measurements with a modulated signal were performed using Keysight M8190A arbitrary waveform generator and Keysight E8267D signal generator as the input signal source. The PA output signal was measured with Keysight UXA N9040A signal analyzer. The cable, probe and pad losses were measured and taken into account in shown results.

Nominal bias of the PA was set to class AB with I_{dQ} = 20 mA. V_{bg} was set to 0 V and V_{g1} to 340 mV. The next gates in the stack were biased to higher values with 900 mV step, resulting in $V_{g2} = V_{g1} + 900\,\text{mV}$ and $V_{g3} = V_{g1} + 1.8\,\text{V}$.

Three bias settings were chosen for comparison. The purpose was to produce the same I_{dQ} with different gate and back-gate combinations. Although back-gates were enabled for all three transistors in the stack, they were biased in unison for simplicity. V_{bg1}, V_{bg2} and V_{bg3} were all set to same value, referred as V_{bg}. The points of comparison were chosen from opposite edges of the back-gate tuning range. With negative back-gate $V_{bg} = -350\,\text{mV}$ the gate voltages were increased in order to get I_{dQ} = 20 mA and so V_{g1} was increased to 370 mV from nominal 340 mV. Similarly with positive back-gate V_{bg} = 2.8 V, V_{g1} was decreased to 110 mV from 340 mV.

B. S-Parameter Measurements

Measured and simulated S11 and S22 curves with nominal bias settings are shown in Fig. 5 a) and b), respectively. From the results it can be seen that the proposed PA input passband matches 3GPP/FR2 band n257 (26.5 GHz-29.5 GHz). S21 with pads was 11.4 dB with 2.5 GHz 0.5 dB bandwidth. In the design test bench transistor stack was layout extracted and transformer-based input and output matching circuits were EM-simulated. In the measurements, frequency responses were shifted compared to what was expected. Simulations suggest that the effect of this on the input matching is quite tolerable. However, it affects the output matching and might be the reason that the measured output power and gain are up to 2 dB lower than estimated with the simulations.

C. Single Tone Measurements

Measured gain, PAE and AM-PM as a function of output power at 28 GHz is shown in Fig. 6. Most notable difference between the bias settings can be seen in gain and AM-PM behaviour. V_{bg} = 0 V and $V_{bg} = -350\,\text{mV}$ settings display almost the same gain values with difference only in the order of 0.1 dB, at most. With the V_{bg} = 2.8 V case the gain has dropped by 0.8 dB from the 11.9 dB reference value. Similarly the AM-PM curves are almost identical between the negative and grounded back-gate settings. With positive back-gate the phase seems to rotate more on the backed off power levels, but ends up with total AM-PM of 5.1°, which is over three degrees less than with other settings. Measured maximum output power of 16.3 dBm was reached with all of the bias settings. With V_{bg} = 2.8 V the said power level was achieved with 0.8 dB less compressed gain. 1-dB compression points for $V_{bg} = -350\,\text{mV}$, 0 V and 2.8 V were 13.3 dBm, 13.5 dBm and 13.9 dBm, respectively. The network analyzer source power was enough to drive the PA into 4 dB compression. Maximum PAE of 23 % was reached with positive back-gate. $V_{bg} = -350\,\text{mV}$ and 0 V came close behind with 22.4 % and 22.7 %.

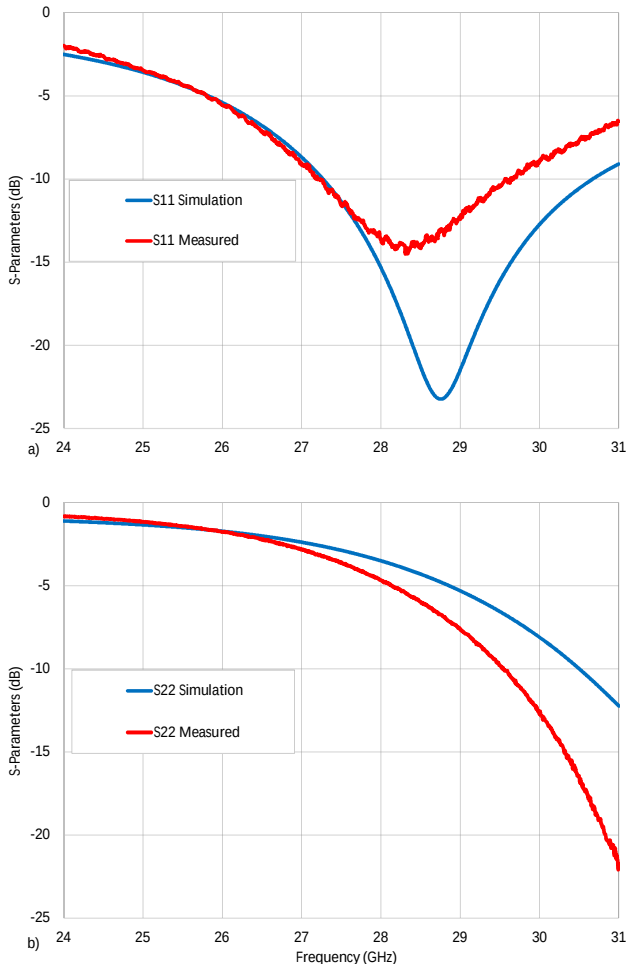

Fig. 5: Measured S-parameters.

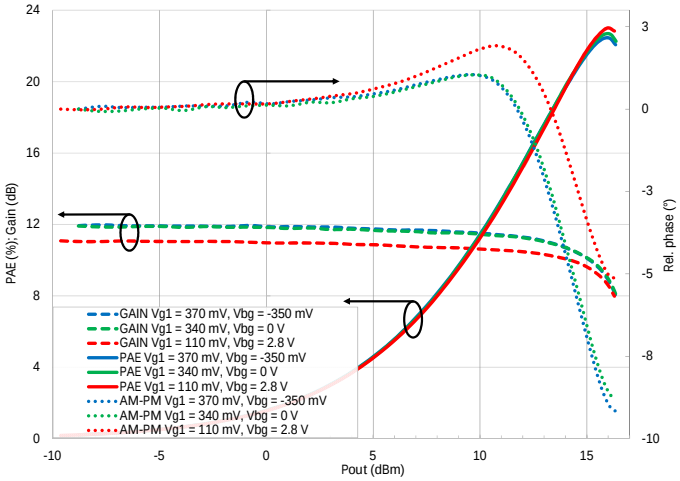

Fig. 6: Single tone measurement results at 28 GHz.

D. Measurements with a Modulated Signal

A 100 MHz 64-QAM 3GPP/NR OFDM signal was used as a test signal. The EVM and ACLR reference levels measured using on-chip Thru were 2 % and −41 dBc, respectively. Fig. 7 a) shows measured EVM and b) ACLRH results as

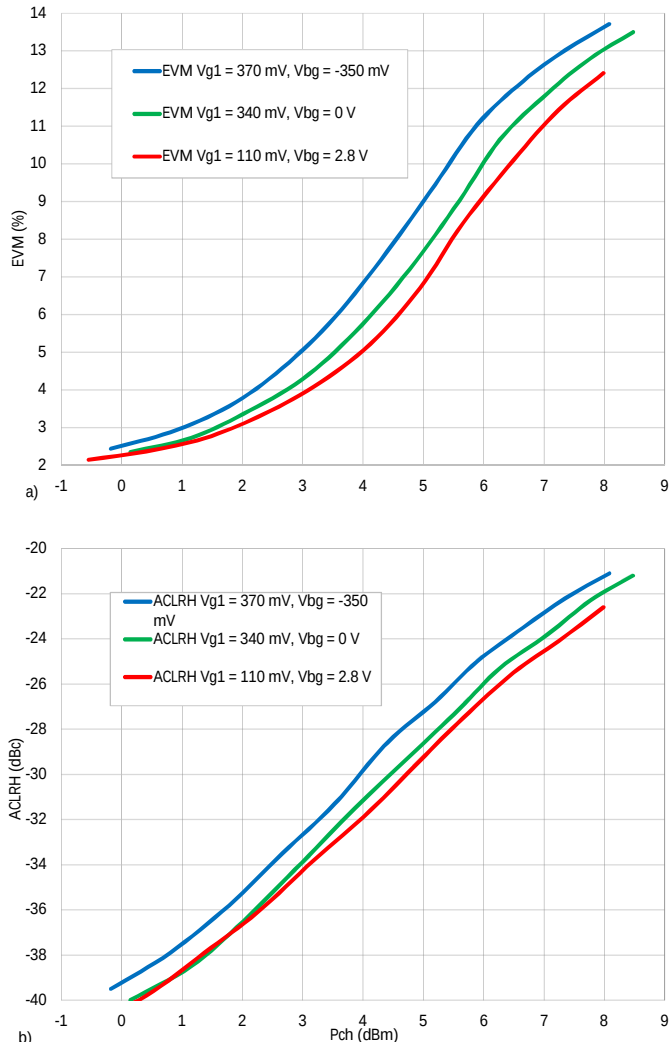

Fig. 7: Measured EVM and ACLRH at 29.45 GHz.

a function of PA output channel power at $29.45\,\mathrm{GHz}$ center frequency. ACLRH, referring upper sideband, performed slightly worse than the lower sideband and that is the reason why only it is depicted on the graph.

V_{bg} = $2.8\,\mathrm{V}$ setting displays better performance both on EVM and ACLR throughout the measurement range. EVM and ACLR limits of $8\,\%$ and $-28\,\mathrm{dBc}$ were used as a benchmark [7]. ACLR was observed to be the more limiting specification and therefore used as a threshold for output power comparison. According to the measurements, V_{bg} = $2.8\,\mathrm{V}$ can reach $5.5\,\mathrm{dBm}$ channel output power P_{ch} with $-28\,\mathrm{dBc}$ ACLR, which is up to $0.8\,\mathrm{dB}$ better than the other settings. EVM and ACLR performance between the bias setting compared are in Table I. The table compares also ACRL and EVM performance at fixed output power, demonstrating back-off properties.

IV. Conclusions

The use of back-gate biasing enabled by $22\,\mathrm{nm}$ CMOS FDSOI technology is demonstrated with a fully integrated three-stack power amplifier. The principle of setting the operating point with back-gate present was analyzed with

TABLE I: ACLR and EVM comparison between the bias settings.

	$V_{bg} = -350\,\mathrm{mV}$	$V_{bg} = 0\,\mathrm{V}$	$V_{bg} = 2.8\,\mathrm{V}$
P_{ch} at $-28\,\mathrm{dBc}$ ACLR	$4.7\,\mathrm{dBm}$	$5.3\,\mathrm{dBm}$	$5.5\,\mathrm{dBm}$
PAE at $-28\,\mathrm{dBc}$ ACLR	$4.5\,\%$	$5\,\%$	$5.2\,\%$
ACLR at $5\,\mathrm{dBm}$ P_{ch}	$-27.3\,\mathrm{dBc}$	$-28.6\,\mathrm{dBc}$	$-29.3\,\mathrm{dBc}$
EVM at $5\,\mathrm{dBm}$ P_{ch}	$9\,\%$	$7.7\,\%$	$6.8\,\%$

a single NFET model and the effect on PA metrics with different bias settings was measured. The PA has active area of $0.07\,\mathrm{mm}^2$ and operates at 3GPP/NR band 257. The use of positive back-bias resulted in maximum measured power of $16.3\,\mathrm{dBm}$ along with peak PAE of $23\,\%$ and 1-dB compression point of $13.9\,\mathrm{dBm}$. The use of lower back-gate bias provided peak measured gain of $11.9\,\mathrm{dB}$ with a trade-off in linear range. The use of positive back-gate bias led to the best performance with a $100\,\mathrm{MHz}$ 64-QAM OFDM signal. $-28\,\mathrm{dBc}$ ACLR was achieved at $5.5\,\mathrm{dBm}$ channel power with PAE = $5.2\,\%$.

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