Design of Multi-Stacked CMOS mm-Wave Power Amplifiers for Phased Array Applications Using Triple-Well Process

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***Abstract*—This paper concerns with the design of multi-stacked CMOS millimeter-wave power amplifiers suitable for phased array front-end applications using triple-well process. The parasitics posed by the triple-well technique are studied and compensated using negative capacitance technique for proper operation. The design technique is evaluated using TSMC 28nm CMOS process at 28GHz operating frequency as a candidate operating band for 5G systems. The results illustrate a power gain of 25dB, 22dBm saturated power, and a maximum 38% PAE along with superior phase alignment between stacks.**

Keywords—CMOS integrated circuits; millimeter-wave integrated circuits; mm-wave power amplifiers; stacked-transistor; deep n-well process; triple-well process; phased-array; 5G.

I. Introduction

Stacking transistors (Fig. 1) were proposed to overcome the issues such as low breakdown level, low output impedance, large parasitics, and low output power provided by a single transistor, when CMOS transistors are utilized as mm-wave power amplifiers (PA) for the next generation of wireless communications systems [1] – [9].

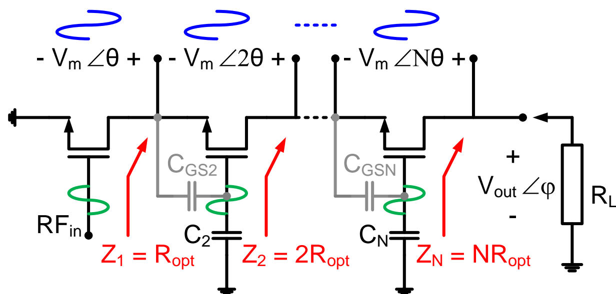

Fig. 1. Typical multi-stacked CMOS PA.

A typical schematic of stacked CMOS PA topology is shown in Fig. 1, which is based on series connection of a common source stage with several common gate stages; the gates of which are not completely bypassed to the ground. Instead, the gate capacitances $C_2 - C_N$ are designed so that the desired optimal load line defined by R_{opt} is guaranteed while a part of signal swing is allowed at the gate nodes. This way, the signal swing across each junction, i.e. V_{DS}, V_{GS}, and V_{DG}, is limited to be within the breakdown constraints. Thus, the overall device signal swing is multiplied by the number of stages, i.e. $V_{out} = NV_{D1}$. This however is not achieved easily due to the fact that the core transistor parasitics are inevitably present, which are very well explained in [3] – [4]. However, this is not the case when it comes to bulk CMOS processes as they pose parasitics, which tend to drastically deteriorate the overall PA performance. Not only that but also, as is explained in the following sections, this will eventually end in PA breakdown. Accordingly, [3] – [4] lack the adequate behavioral parasitic models while the proposed methods explained in [2] – [9] prove insufficient when designing bulk CMOS PAs.

This paper is devoted to design stacked CMOS transistor PAs in bulk CMOS deploying the so-called triple-well/deep n-well process technique and its corresponding issues.

II. Triple-Well CMOS Process

As the linearity of a PA is of prime importance, the very first issue in stacking CMOS transistors is their body effect, which is a strong nonlinear function of voltage across source-bulk junction, i.e. v_{SB}. In order to eliminate this problem, it is required to isolate each transistor by a technique so that their body is isolated from each other and hence the body effect is removed.

Silicon-on-insulator/sapphire (SOI/S) CMOS processes are most extensively used for the mentioned purpose wherein the CMOS transistors are formed in an Si-island manner between each of which there exists SiO_2 insulation. However, such processes pose cost efficiency issues compared to bulk CMOS processes. Therefore, one surmises to use bulk CMOS process technology instead. In order to do that, bulk CMOS vendors provide additional triple-well process in which each transistor can be isolated from the others. This is done using a deep n-well (DNW) implantation followed by deep diffusion. A simplified cross-section of the mentioned technique is shown in Fig. 2.

The body isolation based on the mentioned process technique however poses two issues; a diode and a parasitic capacitance are formed between the DNW and P-well, which must be considered when designing the stacked CMOS PA (Fig. 2).

The effect of the former can be simply minimized by reverse biasing the PW-DNW junction. To remove the body effect the P-well, the bulk of the MOS transistor as well as the anode of the diode, is directly connected to the source. So as to make sure the diode is not conducting, both the NW and DNW should be biased even higher than the highest source voltage of the topmost transistor. Moreover, since the signal at the output may reach $2\times V_{DD}$, there exists a risk of direct conduction for the mentioned diode. Thus, both the NW and DNW are biased at $2\times V_{DD}$ so that the cathode is always at the highest possible voltage level which assures a non-conducting diode.

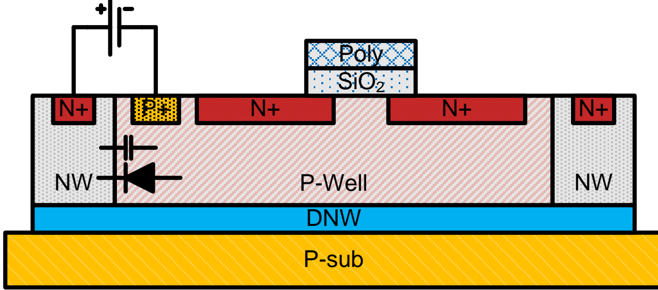

Fig. 2. Simplified cross-section of deep n-well (DNW) process and its most dominant parasitics in bulk CMOS technology.

This, however, is not the case for the latter as it profiles a bias dependent behavior (Fig. 3); the effect of which is analyzed in section III.

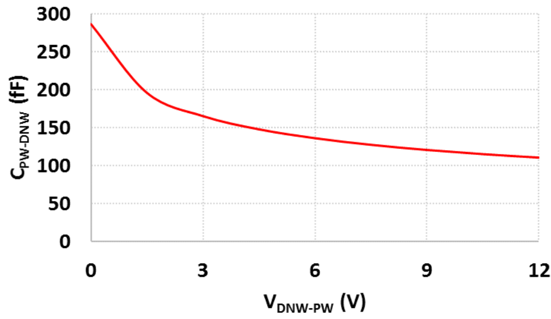

Fig. 3. Bias dependancy of PW-DNW parasitic capacitance.

III. STACKED CMOS PA USING TRIPLE-WELL

As explained earlier the body of each single transistor can be isolated from the others at the cost of a parasitic capacitance between the body of the transistor and the deep n-well. As for the parasitic diode not to conduct, it is reverse biased which means that the $C_{PW\text{-}DNW}$ is shared between a signal ground and the source of each transistor (Fig. 4).

The voltage of the $n+1^{st}$ source node equals nV_{D1} which means that the current of the corresponding $C_{PW\text{-}DNW}$ is $j\omega nV_{D1}C_{PW\text{-}DNW}$ (Fig. 4). This current has no choice but to be sunk from the drain/source of its corresponding MOS. As the gate-source voltages are fixed, the excessive current will force the drain-source voltage to increase proportionally for the required sunk current. This unfortunately increases the risk of breakdown for the upper stacked transistors to a high extent, in a sense that the topmost transistor is more prone to break (Fig. 5).

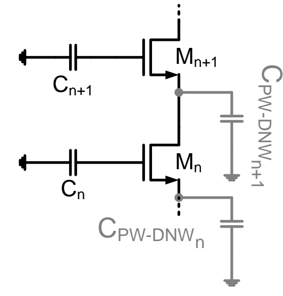

Fig. 4. Presense of pw-dnw capacitance at the source of each transistor.

Even if the structure can survive the breakdown stress, the existence of such a parasitic results in excess phase rotation along the stages which deteriorates the phase alignment between them; hence the overall output power and efficiency will decrease if not compensated properly [3] – [4], [8] – [9]. To do so, an additional mechanism needs to be deployed, which is done through a capacitance feed from the drain back to the source of each common gate stage (see Fig. 6).

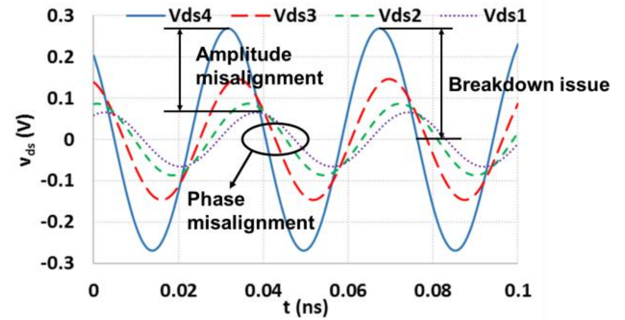

Fig. 5. Improper voltage distribution along the staked MOS PA as a result of $C_{PW\text{-}DNW}$.

Calculating the input admittance of the $n+1^{st}$ stage and equating its real part to $1/(nR_{opt})$, as stated in Fig. 1, results in gate capacitance, C_n, dimensioning rule as follows,

$$C_{n+1} = \frac{C_{gs} + C_{gb} + C_{gd}\left(1 + g_m R_{opt}\right)}{n g_m R_{opt} - 1} \tag{1}$$

which agrees with the proposed dimensioning rules [4] and [7], with an additional C_{gb} term. This seems to be necessary as it may reach to a fraction of the C_{gs} itself.

This however leaves reactive loading, [3], looking both upwards, i.e. Y_{in}, of the $n+1^{st}$ stage and downwards, i.e. Y_{out}, on the nth transistor stage plus the $C_{PW\text{-}DNW}$ which must be compensated. Writing the susceptances Y_{in} and Y_{out} we have

$$\mathrm{Im}(Y_{in_{n+1}}) = \frac{\omega}{n}\left(\frac{C_{gs}+C_{gb}}{g_m R_{opt}} - \left(C_{ds_{n+1}} + C_{db}\right) + nC_{PW-DNW_{n+1}}\right) \tag{2}$$

and

$$\mathrm{Im}(Y_{out_n}) = \frac{\omega}{n}\left(\frac{C_{gd}}{g_m R_{opt}} + C_{ds_n} + C_{db} + C_{gd}\right). \tag{3}$$

As mentioned earlier, it is immediately seen from (2) and (3) that there exists an inconsistency between the imaginary parts of nth and $n+1^{st}$ stages which must be removed.

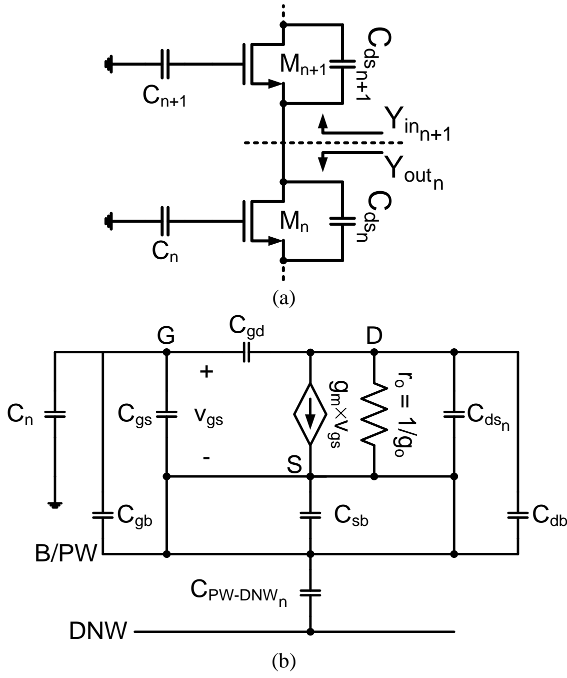

Fig. 6. a) Proposed negative capacitance compensation methodology, b) High-frequency small-signal model of a bulk CMOS transistor along with the effect of deep n-well parasitic and capacitive voltage devider (C_n) and negative capacitance compensator (C_{ds_n}).

Interestingly, (2) explains how the capacitance $C_{ds_{n+1}}$ appears as negative while the other terms of (2) and (3) remain positive with the exception of C_{db}'s which cancel out each other. The mentioned negative capacitance can be deployed to compensate for the remaining reactive parts of each node if properly designed. This is done by equating (2) and (3) and solving for $C_{ds_{n+1}}$. Thus,

$$\frac{\omega}{n}\left(\frac{C_{gs}+C_{gb}}{g_m R_{opt}}-\left(C_{ds_{n+1}}+C_{db}\right)+nC_{PW-DNW_{n+1}}\right) = -\frac{\omega}{n}\left(\frac{C_{gd}}{g_m R_{opt}}+C_{ds_n}+C_{db}+C_{gd}\right) \quad (4)$$

Solving (4) for $C_{ds_{n+1}}$ gives

$$C_{ds_{n+1}}=\frac{C_{gs}+C_{gb}+C_{gd}}{g_m R_{opt}}+C_{gd}+C_{ds_n}+nC_{PW-DNW_{n+1}} \quad (5)$$

with $C_{ds_1}=0$ for $n = 1$.

Dimensioning rules (1) and (5) must be deployed concurrently to guarantee proper phase detuning/alignment along the stacks. Although the calculations were performed for proposed negative capacitance compensation method, the approach can be applied to other detuning techniques without loss of generality. More importantly, $C_{ds_{n+1}}$ can be dimensioned to compensate for more parasitics in order for more phase detuning purposes.

IV. Design Example

In order to verify the proposed design methodology, a 28GHz four-stack CMOS PA was designed and simulated based on TSMC 28nm CMOS technology (Fig. 7). The component values and transistor parameters are listed in Table I.

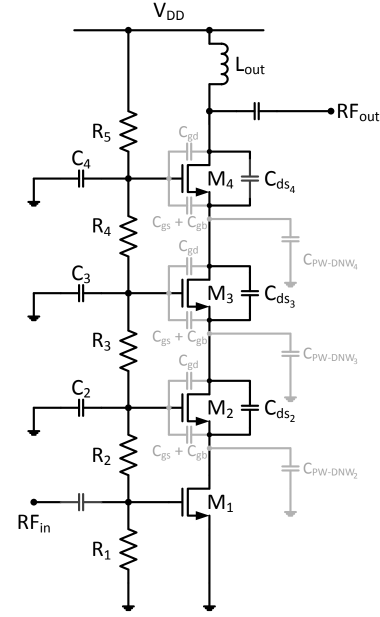

Fig. 7. Simplified schematic of the designed 4-stacked mm-wave PA circuit.

TABLE I. Component Values and Transistor Parameeters

Parameter	Value
V_{DD}	3.6V
g_m	145mS
C_{gb}	17fF
C_{gs}	280fF
C_{gd}	62fF
C_{db}	10fF
C_{PW-DNW}	Fig. 3
C_n	(1)
C_{DSn}	(5)

Fig. 8 illustrates the I-V_{gs} characteristics of the designed 4-stack PA, from which it can be implied that the I-V curves are properly aligned. A proper drain to source voltages, V_{ds}, distribution is expressed in Fig. 9. That is, the overall signal swing is properly distributed across transistor channels that guarantees PA operates appropriately. Compared to Fig. 5, it is seen that after negative capacitance compensation, the V_{ds}'s are totally in-phase and their amplitudes are quite much equal to each other which removes both the breakdown issue and performance degradation problem at the meantime. Also gradual signal swing at each drain node is observed looking at Fig. 10.

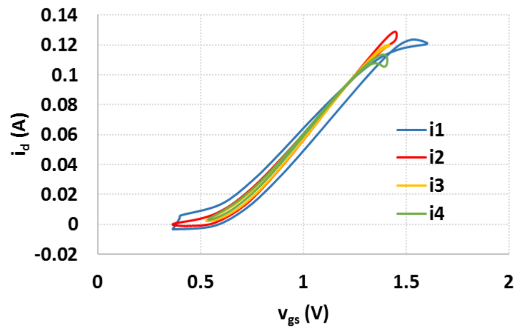

Fig. 8. I-V characteristics of each single transistor in stacked CMOS PA.

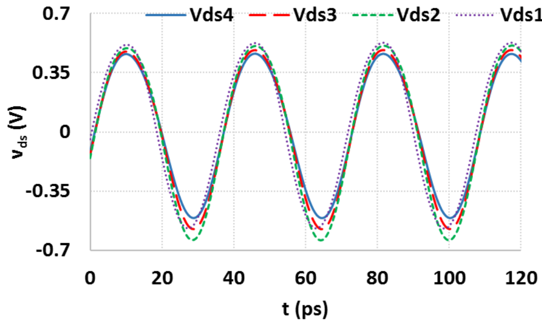

Fig. 9. Voltage distribution along the transistors in the stacked CMOS PA.

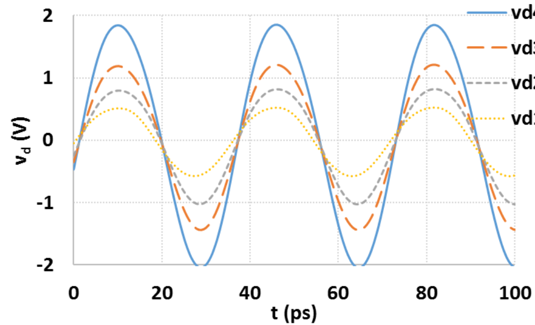

Fig. 10. Increamental drain voltage in the stacked PA.

Simulated s-parameters (Fig. 11) show that both the input and output are well matched at 28GHz with better than -10dB S_{11} and S_{22}. The PA demonstrates a small signal gain of 17dB at the desired frequency. Also an isolation of more than 25dB over the whole bandwidth.

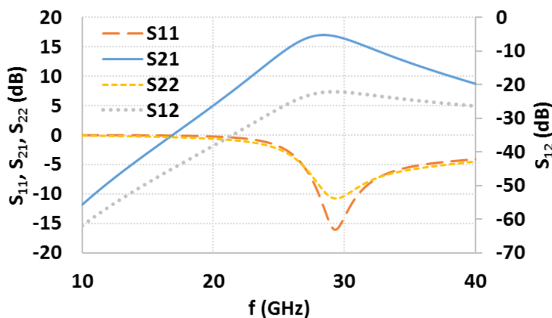

Fig. 11. S-parameters of the designed 4-stack PA

The large signal performance of the device is depicted in Fig. 12. Simulations express a saturated output power of 22dBm, along with 38% power added efficiency and 25dB power gain.

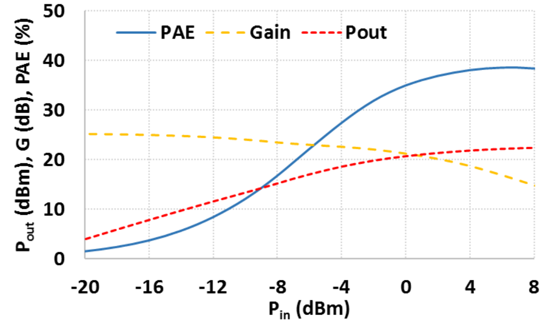

Fig. 12. Overall stacked CMOS PA performance.

V. Conclusion

The design of stacked CMOS transistors based on triple-well process was explored in this study. It was shown how the added deep n-well poses drastic performance degradation as well as serious breakdown problem. The concept of negative capacitance was deployed to compensate for the excess parasitics imposed by the wells, i.e. P-well and DNW. Finally, a design example was presented to show the viability of the technique at 28GHz. The designed PA offered 22dBm P_{sat}, 38% *PAE*, and a G_p of 25dB.

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