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Microelectronics, Nanoelectronics: step behind the red brick wall using the thermal domain

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Abstract

The More-than-Moore Grand Challenge is a hot topic of present day solid state electronics: one way to step behind the "red brick wall" is the 3D heterogeneous integration of different systems with the conventional (standard) CMOS-technology. The aim of this study is to summarize the different bit representation methods, especially possibilities of our new, patented phonsistor (phonon transistor) based thermal-electronic logic system or thermal-electronic logic circuit (TELC). TELC is the first logic gate approach using two different physical quantities, i.e. electrical and thermal for bit representation within one system.

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1. Introduction

All information-related things are represented by „bit"s nowadays: pictures, texts, sounds, environmental parameters (composition or contamination of the air, pressure, and temperature), money (bitcoins). Logic variables (bits) can be represented by many different physical quantities, i.e. mechanical, electrical, photonic, molecular and quantum-state [1] depending on operation mode of the information processing system.

The Moore's law conform exponential technology development has been continuous until now. The collection of physical, technical and economical limitations is usually mentioned as the "red brick wall". The recent technology has not got any methods to step behind it. Moreover some bricks in the red brick wall represent strict and unbreakable rules (atomic distances, thermal noise, and light speed).

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The operation principle of the logic (computing) systems is strongly related to the bit representations. Conventional digital systems are based on electrical signal processing, photonic communication for larger distances, and on optoelectronic/mechanical principles for data output, i.e. displaying and printing.

The first logic (computing) systems were realized using mechanical principles; bits were stored using mechanical quantities in these systems. Abacus, Pascal's calculator are digital, slide rule is an analog mechanical computer. An example for advanced mechanical information storing is a micro-electro-mechanical (MEMS) based system (see the millipede concept [2]). Nano relays [3] and fluidic logic [4] are also mechanical computing systems. Thermal logic [5], [6], quantum computing [7] and spin electronics [8] are emerging technologies. However, these kind of computing principles are too far from the standard CMOS technology and seem to be incompatible with it.

The minimum energy, which is necessary to process and store one bit is related to the thermodynamical (noise), quantum mechanical (Heisenberg uncertainty) and heat transfer (system cooling) limits [9]. These items are really hard bricks in the above mentioned red brick wall.

The bit transfer is connected with energy transfer, which can be generally described by continuity equations. These equations are mathematically second order linear differential equations composed from the second derivative by space coordinates and first derivative by time of some information carrier quantity (Q):

$$\alpha \frac{\partial}{\partial x^2} Q \approx \frac{\partial}{\partial t} Q \tag{1}$$

where α is a material-specific coefficient depending on the physical nature of Q and material properties of a given system, see Table 1. for examples. Some other second order differential equations are also included in that table, where the time derivative is zero (static situation for beam deflection and potential due to space charge). Solutions of these kind of equations usually result in characteristic distances defining the scale down limits, and characteristic times defining the speed limits for the information transfer. The recent computer technology is based on the advanced CMOS technology. The continuous scaling down resulted in extremely small size and high speed systems. These systems are very near to the "red brick wall". Further development is almost impossible using the conventional scaling down methods [10].

Table 1. Basic physical effects, equations and related devices.

Equation	Q	α	Characteristic distance	Characteristic time	Related device types
Equation of the elastic curve	Beam deflection	Modulus of elasticity, moment of inertia of the cross section / bending moment	Remarkable deformed domain, square root of α	-	Microrelay, nanorelay
Poisson equation	Potential in the presence of space charge	Dielectric constant	Depletion layer width, Deby length	-	Field effect devices
Diffusion equation	Minority carrier concentration	Diffusion constant of the minority carriers	Diffusion length	Minority carrier lifetime	Bipolar devices
Differential equation for voltage pulse propagation on RC transmission line	Potential among a distributed RC line	Square resistance – capacitance product	Electric charge diffusion length	Time constant	IC metallization
Heat equation	Temperature	Thermal diffusivity	Thermal diffusion length	Thermal time constant	Thermal devices
Schrödinger equation	Wave function	Planck constant/electron mass	Tunneling distance	Transit time	Nanoelectronic devices

2. Thermal-electronic operation

The thermal-electronic operation is a new principle for logic gate and logic system realization based on thermally sensitive electrical elements (pn junctions, temperature controlled resistors) [11]. In the thermal-electrical integrated circuit both the electrical and thermal signals are treated as logic variables. The thermally sensitive switch integrated with a controllable heating element can be considered as a new thermal-electronic device: phonon transistor or "phonsistor" [11].

It has been demonstrated earlier that using the metal-insulator transition (MIT) or semiconductor-metal transition (smt) resistors (R_{MIT}) results in high voltage gain (A), because of their high derivative around the phase transition temperature:

$$A = \frac{\partial V_{out}}{\partial V_{in}} = I \frac{\partial R_{MIT}(T)}{\partial T} \cdot \frac{\partial T}{\partial V_{in}} = 2 V_{in} I \cdot \frac{\partial R_{MIT}}{\partial T} \cdot \frac{R_{th}}{R_{in}} \tag{2}$$

where R_{in} is the input electrical resistance of the above mentioned controllable heating element, R_{th} is the thermal resistance to the environment, T is the temperature, I is the current of power supply. Considering the large signal behaviour, the MIT resistor has got a thyristor-like switching characteristic due to negative temperature coefficient and self-heating, see Fig. 1. Moreover the negative temperature coefficient may result in inhomogeneous current distribution, *i.e.* a narrow metallic conductive channel, thus the thermal resistance (R_{th}) increases. The higher thermal resistance value helps to keep the low electrical resistance (ON) state, as lower electric power dissipation is enough to reach and keep the transition temperature among the conducting channel.

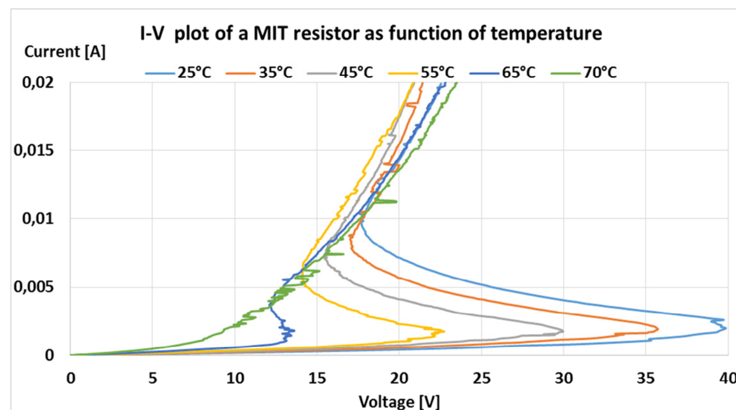

Fig. 1. I-V characteristics of a VO_2 MIT resistor at different environmental temperature

3. Practical realization of the thermal-electronic device

The thermal-electronic operation is demonstrated on a VO_2 based lateral phonsistor (TELC) structure realized by thin (~50 nm) RF cathode sputtered VO_2 (MIT) and Pt metal layers on a ~1.5 mm size oxidized silicon substrate. Fig.2. shows the schematic arrangement and layout of the system. The frame-like metallization completely separates the input and output resistors from each other; there is only thermal interaction between them.

The input and output characteristics of thermally coupled VO_2 resistors are plotted in Fig. 3. It is easy to recognize that the system is basically a NOR gate: either of the excited input resistors may help to switch the output. However, using shorter electrical exciting pulses than the thermal time constant of the system, or lower exciting

power, the NAND operation can also be demonstrated. In that case more than one input resistor should be excited injecting enough energy into the system to switch on the output, as it has been discussed earlier [12].

The thermal interaction between thermally coupled MIT resistors makes the situation difficult: all resistances depend on the temperature, which is proportional with the sum of the input and output electric power dissipated on the whole system. Therefore the electrical characterization of the thermally coupled MIT resistors is more difficult, compared to the other simple two-port systems. Let us consider, for example the (0)-(1)-(2)-(3)-(4) switching procedure on the output I-V curve in the Fig. 3., where both the input and output resistors were excited. The output resistor starts to switch at lower voltage due to a moderate input excitation (1), the output resistor is in low impedance metallic state (2), the temperature is high enough to switch on the input resistor too (3), both resistors are in low impedance state (4). Without input excitation (I_{in}=0) only the output resistor switches on at higher voltage, while at higher input excitation the input and output switching process cannot be separated on the output I-V plot.

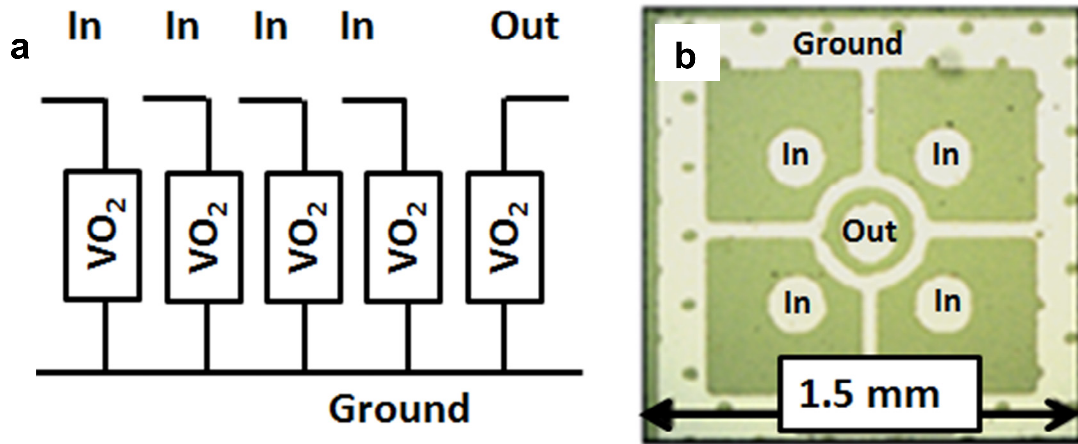

Fig. 2. (a) thermally coupled resistors for modeling the phonsistor operation; (b) layout with metal electrodes

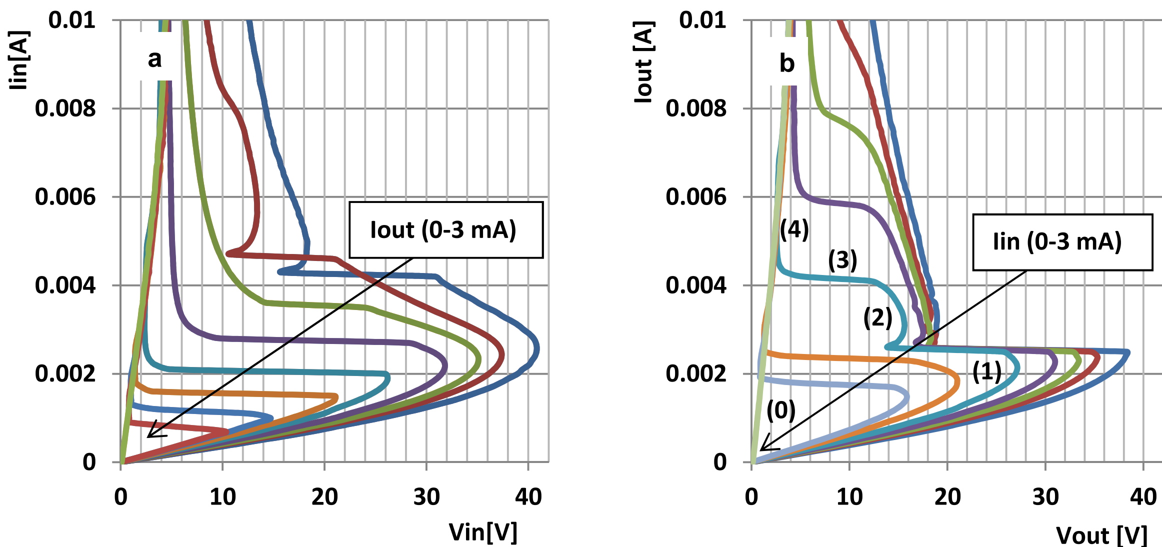

Fig. 3. (a) input and (b) output I-V characteristics of the phonsistor (a set of thermally coupled VO_2 resistors)

4. CMOS and thermal-electronic device

The relationship between the CMOS and thermal-electronic device (TELC) has got two aspects. The first is compatibility, the second is scalability. The MIT based phonsistor is an extremely simple bulk type device, it consists of only thermally coupled lateral or vertical VO_2 resistors with metal contacts. These kinds of resistors can probably be incorporated into a CMOS metallization system. One possibility is to deposit VO_2 plugs into vias or contact windows instead of metal, this method results in a vertical resistor as small as the diameter of holes in the dielectric layer. The thermal and electric bit representations give an extra chance for information exchange between CMOS and TELC, i.e. the TELC can be controlled by thermal dissipation of the CMOS too.

Concerning the scalability (see Table 2.), it should be pointed out that the CMOS is a much more difficult system compared to the thermal-electronic device: all CMOS transistors are surface type devices containing a number of different doping materials, junctions, contacts, and interfaces. Scale down limits for the CMOS device are related to thicknesses of depletion layers and tunnel currents; the direct tunnel distance is about 2 nm for the case of moderate potential barrier height. Moreover, to build an ”*n*” input CMOS gate 2*n* transistors are necessary.

As the MIT device is only a bulk VO_2 resistor with contacts, due to its simplicity the scaling down seems to be easier. However, some scale down limits still exists: the tunnel current, MIT effect size dependence, electron free path and phonon free path. The MIT effect has been demonstrated on 10 nm VO_2 crystalline [13]. This size can now be considered as a limit of scaling down for the TELC. The switched on VO_2 resistor keeps the information thermally, even after the power supply (clock signal) went down, thus it has got more functionality compared to the CMOS gate. The “*n*” input TELC gate can be built from *n* input resistors thermally coupled with a MIT resistor. If the MIT resistor is powered through a pull up resistor than the total number of components are *n*+2. However, the pull up resistor may act as one of the input resistors of another gate in the system, thus the final number of components are less than *n*+2.

Table 2. Comparing the CMOS and TELC gate limitations

Parameters / Technology	Geometry, volume	Power supply	Clock frequency	Number of components
Recent CMOS gate properties:	(14+14)x50x50 = 70000 nm^3	0.8-0.7 V	4 GHz	2*n* (NMOS-PMOS)
Estimated theoretical limits for CMOS:	(7+7)x30x30 = 12600 nm^3	0.5 V	6+(?) GHz	2*n* (NMOS-PMOS)
Estimated limits for TELC:	10x10x30 = 3000 nm^3	0.4- 0.2 V	10 Ghz	<*n*+2 (functional device with memory)

The TELC scaling down has been discussed earlier [14]. The characteristic dimension for thermal transport process is the thermal diffusion length (see Table 1. too)

$$L_{th} = \sqrt{\alpha t} \quad (3)$$

where α is the thermal diffusivity, a material-specific quantity depending on the thermal conductivity, the mass density, and the specific heat capacity. The thermal diffusion length defines the volume to be heated up to start the MIT switching process. The heat capacitance is proportional with the volume, i.e. the third power of the linear size, while the thermal conductance is proportional with the second power of the size, thus the thermal time constant scales down linearly with the geometrical dimensions. In the case of submicron size domain thermal time constant values can be comparable with electrical time constants.

Scaling down near to the phonon free path or electron free path may result in extremely fast switch, as the heat transfer between the dissipating element and the MIT resistor may be faster, and hot electrons may thermalize directly in the MIT resistor; there is no diffusive heat transport in that case.

Conclusion

The thermal-electronic logic is the first and until now unique system with two different kind of physical bit representations. Thermally driven MIT switches were patented earlier [15], but the temperature was not treated as logic state and the heat transfer was not considered as information carrier in those systems. More logic variables (voltage, temperature, mechanical stress, strain etc.) included in one system may result in higher complexity and functionality; however the design and modeling of these systems will be extremely difficult.

The thermal-electronic logic circuit seems to be compatible with the traditional CMOS technology. The hybrid CMOS-TELC micro- or nanosystem could be realized by filling up some parts of vias with metal-insulator transition capable material. The temperature sensitive MIT resistor can read the electric state of a MOS device below, without galvanic connection resulting in extra path for information transfer.

Due to its extremely simple structure, fewer components and smaller size the TELC may help to step behind the red brick wall. Concerning the characteristic volume of the TELC gate, it can be a half order of magnitude less than the smallest CMOS gate (see Table 2., the basis of the estimation is the gate length of the scaled down MOS devices and the smallest MIT capable crystalline size).

The "phononics", i.e. thermal transistors and thermal logic [5] described by Lei Wang and Baowen Li is not connected to thermal electronics. They have succeeded in building diodes and transistors that manipulate or control heat flow. However their concept for thermal transistors and hypothetic thermal logic is not based on semiconductor-metal transition, thus it completely differs from ours. Same holds for the "Near-Field Thermal Transistor" [6], where the radiative heat transport (infrared radiation) is controlled by a MIT plate.

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