

# *A Low Noise Front End Trans-Impedance Amplifier Channel for a Pulsed Time-Of-Flight Laser Radar*

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**Abstract**— A low noise front end trans-impedance amplifier for a pulsed time-of-flight laser range finder receiver is presented. The architecture is based on unipolar-to-bipolar pulse shaping immediately at the input of the receiver channel, where the received unipolar current pulse is converted to a bipolar current to be fed to the trans-impedance amplifier (TIA). An extensively wide dynamic range is achieved using the proposed pulse shaping scheme and TIA realization. As the timing point is located at the first zero crossing point of the bipolar signal, the non-idealities of the TIA have little effect on it. Simulations show the walk error of the TIA channel to be less than  $\pm 50$ ps in the dynamic range 1:100000. The input-referred noise current and bandwidth are 72.5nA and 415MHz, respectively.

**Keywords**—*time-of-flight; trans-impedance amplifier (TIA); pulse shaping circuit; walk error*

## I. INTRODUCTION

Optical distance measurement methods can technically be categorized into three groups: interferometry, triangulation, and Time-Of-Fight (TOF) [1]. The pulsed TOF laser distance measuring technique refers to the time it takes for a light pulse to travel from the transmitter to the observed object and back to the receiver at the speed of light (roughly  $c=30$ cm/ns) [1]. This technique can achieve millimeter-level distance measurement accuracy in a range of several tens of meters to non-cooperative targets [2]. TOF optical receivers have wide applications in industry, traffic monitoring, gaming, medical imaging, security, advertising, aids for visually impaired persons, vehicle safety, etc.

A TOF system typically includes a laser pulse transmitter, optics, a photodetector, a receiver channel and a time interval measurement unit (TDC). The main sources of inaccuracy in laser range finders are noise-generated timing jitter, timing walk error, nonlinearity and drift with supply voltage and temperature [1]. Jitter in the timing point determines mainly the precision of the range measurement and is proportional to the RMS noise of the receiver and inversely proportional to the slope of the timing pulse at the moment of timing [3, 4]. Walk error, which is the systematic deviation of the timing point with pulse amplitude variations, is caused by either variations in the pulse rise time (geometrical walk error) or changes in the electronic delay in the receiver channel [4, 5].

Several circuit techniques for implementing a precise TOF receiver have been proposed in the literature. The simplest method, known as leading edge detection, compares the

rising edge of the received pulse with a threshold voltage level. However, it suffers from considerable walk error, as the reflected pulse varies over a wide range of 1:100 000 and the rising slope is proportional to the amplitude of the received pulse. To reduce walk error in receivers of this type, compensation techniques such as pulse width [6] or rising/falling slope measurement [7] have been proposed in the literature. Nonetheless, these compensations depend on the exact pulse shape, which may require a complicated calibration procedure for their effective utilization.

Another method, known as linear range detection, adopts gain control to avoid the receiver from being saturated therefore the geometrical walk error is avoided [2]. However, this technique increases complexity of the circuit and the duration of the time interval measurement. Furthermore, the dynamic range (DR) is limited because the signal is not allowed to exceed the linear range of the amplifier channel.

Another technique for improving both the DR and the timing error is to reshape the arrived pulse to a bipolar signal at the input, in such a way that the timing point is placed at the first zero crossing point of the converted signal. As a result, the clipping of the signal at large amplitudes has only a minor effect on the timing point because the receiver channel returns to the linear region in the vicinity of the zero crossing point if it is fast enough to recover from saturation [5]. Although two different implementations of pulse shaping are proposed in [5, 8], the performance achieved is limited. In [5] the RLC pulse shaper adds extra noise at the input of the receiver channel and thus limits both DR and the minimum detectable signal, while in [8] the RC pulse shaper is placed at the output of the trans-impedance preamplifier, and thus its DR is limited by that of the preamplifier.

This paper presents a new pulse shaping circuit to be combined with the TIA. The aim of this work is to develop a low noise solution for extracting the timing point within a wide DR. This front end TIA is intended for use as a part of a TOF laser receiver channel in which input pulses of around 1ns full width at half maximum (FWHM) will be detected using an avalanche photodiode (APD). The paper is organized as follows. The proposed technique and its circuit realization are presented and analyzed in Section II, Simulation results are shown in Section III and conclusions are given in Section IV.

## II. THE TRANS-IMPEDANCE CHANNEL

### A. Pulse shaping Circuit

The proposed pulse shaping circuit, the input photodiode and a block comprising the TIA, are shown in Fig. 1. The photodiode capacitor can be as large as 0.5pF. No resistor is used to bias the photodiode. Furthermore, the front end resistor, which is critical for damping the oscillation generated by the LC network, is implemented using the input resistance of the TIA. This is an interesting feature of the proposed structure which eliminates the need for a relatively small resistor right at the input of the receiver channel, leading to an improvement in the noise performance of the whole receiver channel. The values of the pulse shaping components are chosen based on the input pulse specifications, the transient output signal requirements, the bandwidth and the noise requirements of the TIA. Since the input pulse has a width of 1ns FWHM, the rise time of the pulse is approximately the same, thus, in the light of (1), a bandwidth of around 400MHz is needed [2].

$$BW = \frac{0.35 \text{ to } 0.4}{t_{rise}} \quad (1)$$

As there is no direct control over the photodiode capacitance and parasitic capacitances of the TIA input, the only two parameters to adjust are L and R1. Even though the size of the TIA input transistor determines the input parasitic capacitances, its dimension is selected based on several issues such as the required trans-impedance gain, the bandwidth and the noise.

The amplitude of the output current ( $I_{out}$  in Fig. 1(b)) is important because it is compared with the total input RMS noise. For a precise measurement, a minimum SNR of 5 to 10 is mandatory. A small inductor steers more current to the ground, while a very large inductor limits the bandwidth of the amplifier channel. Hence, considering the bandwidth and the time domain response, an inductance of 1.8 $\mu$ H is chosen here.

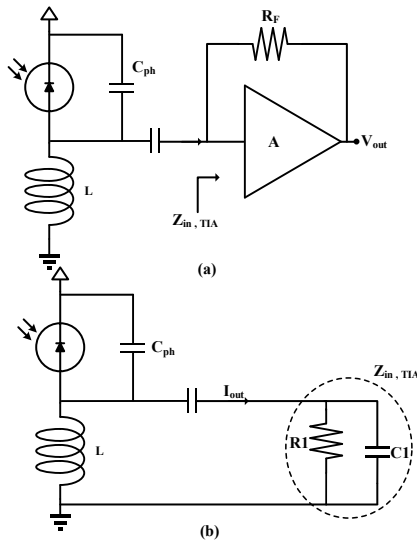


Fig. 1. Proposed front end TIA channel combined with pulse shaping circuit

The input resistance of the TIA ( $R_I$ ) is  $R_F/(A_0 + 1)$ , where  $A_0$  is the voltage gain of the core amplifier. For a flat AC response in the pulse shaping output and the target bandwidth a resistance of around 400 $\Omega$  to 600 $\Omega$  is required. The value of the feedback resistor and core amplifier gain are chosen based on the noise and bandwidth limitations. It is discussed in more detail in section B-3.

### B. TIA

#### 1) General Considerations

A basic block model for the TIA that converts the unipolar current to an amplified voltage in its output is shown in Fig. 1(a). The core amplifier (A) is an inverting voltage amplifier. The feedback resistor builds up a path to convey the current from the pulse shaping unit to the output of the TIA, acting in such a way that the TIA input node remains in virtual ground (for the TIA linear region). The typical frequency response of the open loop circuit, including pulse shaping unit, is shown in Fig. 2. The high-frequency pole ( $\omega_2$ ) is due to the amplifier itself, and the low-frequency pole at  $\omega_1$  is due to the input circuitry. As the input components ( $L$ ,  $C_{ph}$ ) and the TIA input impedance form a parallel RLC circuit, the frequency of this pole is:

$$\omega_1 = \frac{1}{2R_FC_T} + \sqrt{\frac{1}{LC_T} + \left(\frac{1}{2R_FC_T}\right)^2} \quad (2)$$

where  $C_T = C_{Ph} + C_{in,TIA}$ . Given this amplifier model, the closed loop trans-impedance can be calculated as follows:

$$Z_T(s) = -\frac{A_0\omega_2 s}{s^3 + \left(\omega_2 + \frac{1}{R_FC_T}\right)s^2 + \left(\frac{A_0+1}{R_FC_T}\omega_2 + \frac{1}{LC_T}\right)s + \frac{\omega_2}{LC_T}} \quad (3)$$

Simulation of (3) shows that, for a maximally flat frequency response, we should have:

$$\omega_2 \geq 2\omega_u \approx \frac{A_0}{R_FC_T} + \sqrt{\frac{4}{LC_T} + \left(\frac{A_0}{R_FC_T}\right)^2} \quad (4)$$

where  $\omega_u$  is the unity gain frequency. The overall bandwidth of the TIA channel is perfectly approximated as:

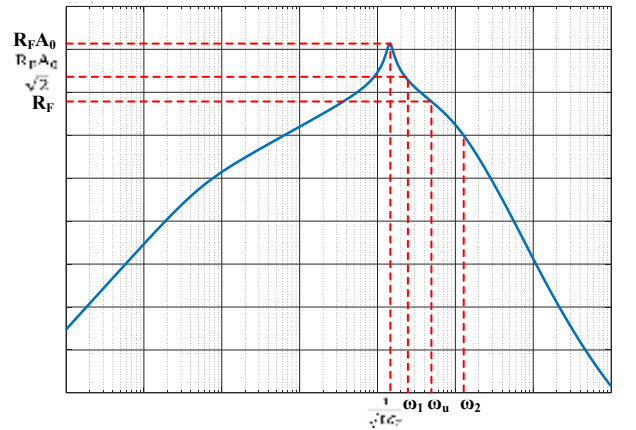


Fig. 2. Typical open loop frequency response of the TIA channel

$$\omega_{-3dB} \cong \frac{A_0+1}{2R_F C_T} + \sqrt{\frac{1}{LC_T} + \left(\frac{A_0+1}{2R_F C_T}\right)^2} \quad (5)$$

### 2) Circuit realization

The primary realization of the TIA circuit is shown in Fig. 3. The core amplifier consists of a cascode stage at the input as the gain stage and two source follower stages as buffers. The transistor  $MP1$  acts as a current source for biasing the input transistor at a higher DC current to boost the  $g_{m1}$ . Thanks to this transistor a larger  $R_L$  can be chosen, which is beneficial for both the gain and noise specifications, even though  $MP1$  adds some noise. The cascode transistor ( $M2$ ) has a key role in canceling the miller effect of the  $C_{DG1}$  and increasing the output resistance seen from its drain. As a result, we have more control over the gain and more gain as well. The first buffer used in feedback loop acts as a level shifter for proper biasing of the input transistor. Two buffers have been chosen to isolate the feedback path from the output loading effects, thus improving the stability of the circuit [9]. Besides, adopting two buffers decreases the walk error too.

The first pole of the proposed TIA core amplifier is as presented in (2), and the second pole is:

$$\omega_2 = \frac{1}{R_L C_X} \quad (6)$$

where,  $C_X = C_{DG2} + C_{GD3} + C_{GD4} + \alpha(C_{GS3} + C_{GS4})$  and  $\alpha$  is a constant less than one. To avoid ringing in the step response, the frequency of this pole should comply with (4).

### 3) Noise analysis:

The low-frequency input referred noise of the TIA is as follows:

$$\frac{i_{n,in,TIA}^2}{4KT} = \frac{1}{R_F} + \frac{V_{n,in,core}^2}{R_F^2} = \frac{1}{R_F} + \frac{1}{R_F^2} \left( \frac{\gamma(g_{m,N1} + g_{m,P1})}{g_{m,N1}^2} + \frac{1}{g_{m,N1}^2 R_L} + \frac{\gamma(g_{m,N3} + g_{m,N4})}{g_{m,N3}^2 g_{m,N1}^2 R_L} + \frac{\gamma(g_{m,N5} + g_{m,N6})}{g_{m,N5}^2 g_{m,N1}^2 R_L} \right) \quad (7)$$

where we assume the gain in the buffers is one and neglect the loading effect of the feedback resistor on the core amplifier [9].

It can be seen from (7) that a large  $R_F$  suppresses both its noise and that of the core amplifier. Hence, as far as the bandwidth limitation allows, a large feedback resistor should be chosen. Meanwhile, the required damping resistor of the pulse shaping circuit and also the maximum achievable gain using one cascode stage should be considered.

A model for high-frequency noise for shunt feedback TIAs that takes into account the input capacitance of the TIA and compares it with the photodiode capacitance is suggested in [10], where it is concluded that in order to deliver a high signal-to-noise ratio or achieve a low input referred noise level, the capacitance seen at the input of the TIA should be same as that of the photodiode. This is hard to realize, however, because the photodiode capacitance is very large, and choosing device dimensions that satisfy this condition, will suppress the bandwidth even more. It is suggested in [11] that the input capacitance can be chosen over a wide range from  $0.2C_{ph}$  to  $2C_{ph}$ . These observations are also

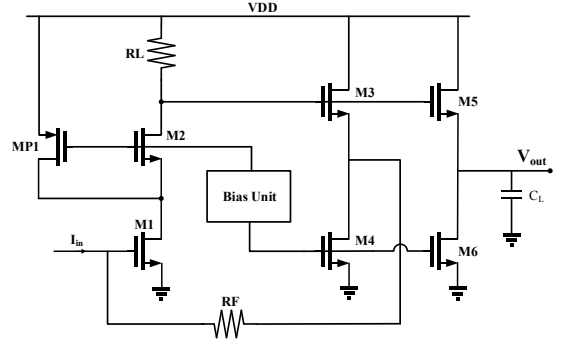


Fig. 3. Primary transistor level realization of the TIA

applicable to our proposed circuit, because at high enough frequencies we can replace the inductor with an open circuit, so that the TIA “see” the photodiode capacitance immediately at its input.

### 4) The proposed TIA

Simulation of the TIA channel (Fig. 1(a)) using the circuit proposed in Fig. 3 shows that the trans-impedance channel works well for the linear region of the TIA (input currents of  $1\mu A$ - $250\mu A$ ), and that the walk error is as low as 14ps. This operating range is too narrow for our application. However, and exceeding the TIA linear region will cause two phenomena to occur. First, the zero crossing point deviation will increase expeditiously, which directly leads to higher walk error and second, the output signal will tend to oscillate, possibly because when the TIA becomes saturated, the input resistance increases from  $R_F/(A+1)$  ( $500\Omega$  in our design) to  $R_F$  ( $10K\Omega$ ) so that damping does not occur and the whole signal is corrupted. To solve this problem, there should be a mechanism to protect the TIA from being deeply saturated, or, equivalently, speed up the process of returning to the linear region. The solution proposed here is shown in Fig. 4. Two auxiliary transistors ( $M_{NF}$ ,  $M_{PF}$ ) are added to the feedback loop. These auxiliary transistors function in the manner of class B stage. For small input currents,  $|V_{GS-MNF,MPF}| \leq |V_{TH}|$  and the two transistors are off, or more precisely they are in the sub-threshold region and have very little effect on the performance of the TIA. As the input increases, the two transistors eventually turn on, and source the current from  $V_{DD}$  ( $M_{NF}$ ) or sink it to the

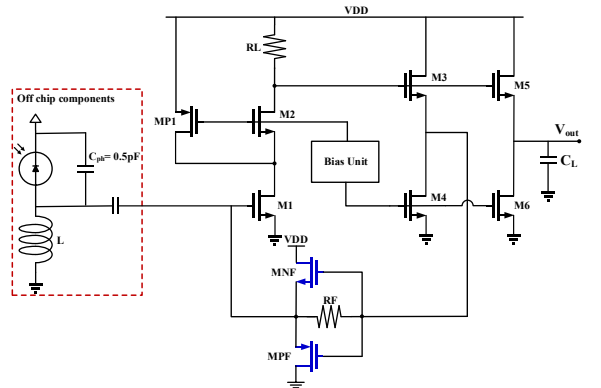


Fig. 4. Proposed TIA front end

ground ( $M_{PF}$ ). The larger the input current is, the more current the transistors steer. As the only important information in the arrived current signal is its zero crossing point generated by pulse shaping, large amounts of input currents can be processed through this amplifier channel. These two transistors have no effect on the low frequency noise performance of the TIA, because they carry no DC bias currents. The parasitic capacitances seen in the source of these two transistors are added to the input node capacitance, and even though they suppress the bandwidth slightly, the high frequency noise performance will be improved, as discussed in section B-3.

### III. SIMULATION RESULTS

The circuit has been simulated using 0.35 $\mu$ m CMOS AMS standard technology in Cadence environment. The circuit draws 3.7mA DC current from a 3.3V bias voltage. The open loop voltage gain was set to 18 and the input device dimensions of the TIA are large enough to make the input capacitance greater than  $0.2C_{ph}$ . The device dimensions and DC bias currents of the proposed TIA are shown in table I and the walk error of the proposed TIA channel for amplitudes between 1 $\mu$ A and 100mA (i.e. over the whole range) is shown in Fig. 5. The walk error for this wide DR is less than  $\pm 50$ ps. The frequency response shows the overall ac trans-impedance gain to be 79.16dB $\Omega$  or 9k $\Omega$  and the bandwidth of 415MHz. The total RMS input-referred noise current is 72.5nA. A summary of the simulation results is given in Table II.

TABLE I. DEVICE DIMENSIONS AND BIAS CURRENTS OF THE PROPOSED TIA

parameter	W/L ( $\mu$ m/ $\mu$ m)	DC current (mA)	parameter	value
M1	70/0.35	2.4	L ( $\mu$ H)	1.8
M2	80/0.35	0.6		
M3	80/0.35	1		
M4	35/0.35	1	R <sub>L</sub> (K $\Omega$ )	2.1
M5	20/0.35	0.31		
M6	10/0.35	0.31		
MP1	60/0.7	1.8	R <sub>F</sub> (K $\Omega$ )	10
MNF	60/0.35	0		
MNP	15/0.35	0		

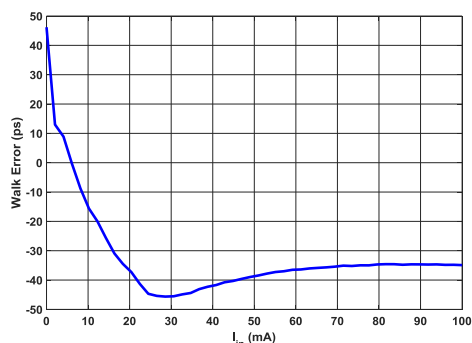


Fig. 5. Output Walk error

TABLE II. SUMMARY OF THE SIMULATION RESULTS

Specification	Simulation results
Process	0.35 $\mu$ m CMOS
AC trans impedance gain	79.16dB
Bandwidth	415MHz
Input referred RMS noise current	72.5nA
walk error	$\pm 46$ ps
Power consumption	12.21mW

### IV. CONCLUSION

A new pulse shaping circuit and TIA for a pulsed TOF receiver channel are presented. The circuit is designed for 1ns FWHM input pulse, and a walk error of less than  $\pm 50$ ps is achieved within a signal range of 1:100000. This wide DR is obtained thanks to the low noise pulse shaping technique and modified shunt feedback TIA. This circuit is a part of a TOF receiver channel which will be designed and fabricated in 0.35 $\mu$ m CMOS technology.

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