A Fully Integrated 13 GHz CMOS SOI stacked Power Amplifier for 5G Wireless Systems

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***Abstract*—This paper presents a fully integrated, four stack power amplifier for 5G wireless systems. The frequency of operation is tunable from $12\,\mathrm{GHz}$ to $14\,\mathrm{GHz}$, with a maximum 3 dB bandwidth of $1\,\mathrm{GHz}$ and a maximum possible gain of $35\,\mathrm{dB}$. The circuit is designed and fabricated using $45\,\mathrm{nm}$ CMOS SOI technology. Maximum RF output power, power-added efficiency (PAE) and output 1 dB compression point under maximum bandwidth configuration are $17.7\,\mathrm{dBm}$, $23.2\,\%$ and $12.3\,\mathrm{dBm}$, respectively, achieved at $13.7\,\mathrm{GHz}$.**

***Keywords*—CMOS, SOI, RF, stacked power amplifier, PA, wireless communications, 5G.**

I. Introduction

To achieve higher data rates promised by the fifth generation of wireless systems, wide band systems operating at centimeter or millimeter wave (mmWave) frequencies are required [1]. In addition to wider bandwidths and higher operating frequencies, they will also incorporate massive parallelism in the form of massive multiple-input multiple-output (MIMO) systems and phased arrays [1]–[3].

In a massive MIMO transmitter, the output power levels required at each antenna decreases proportionally to the number of antennas. Hence, instead of splitting the power to each antenna branch from one high power PA, it is possible to use a low power PA in each antenna chain. Since the number of PAs will increase significantly compared to the previous generation solutions, several issues such as, cost, size, complexity and efficiency, needs to be optimized. Here, a CMOS PA is a quite tempting alternative as it provides reasonable RF power at millimeter waves, is simple and can act both as a driver for an external PA, or even a main PA for picocell applications [4]–[7].

In this paper, we describe a four stack PA implemented in $45\,\mathrm{nm}$ CMOS SOI process. The PA consists of two stages, a cascode driver stage followed by a four stack PA stage. The PA incorporates exhaustive digital controls which allows to tune the frequency of operation from $12\,\mathrm{GHz}$–$14\,\mathrm{GHz}$ along with the possibility of trading the gain with bandwidth. The PA provides a peak gain of $35\,\mathrm{dB}$ measured at $12.2\,\mathrm{GHz}$. The available bandwidth for this configuration is $100\,\mathrm{MHz}$. By modifying the digital configuration, the bandwidth can be enhanced to $1000\,\mathrm{MHz}$. The output saturated power measured for this configuration is $17.7\,\mathrm{dBm}$ and occurs at $13.7\,\mathrm{GHz}$.

The organization of this paper is as follows, in Section II circuit design for all the related blocks is described, followed by the measurement results in Section III. Conclusions are drawn in Section IV.

II. Circuit Design

A. Cascode Driver

The first stage of the design is a cascode driver stage, shown in Fig. 1. A variable capacitor C_1 and inductor L_1 forms up a tunable input resonator, which performs the following two important tasks. The first task is governing the frequency response of the stage. By changing the value of C_1, frequency response of the stage can be altered. Furthermore, as the input resonator is determining the frequency response, it allows the output DC feed and DC coupling to be chosen more freely. The second task is related to the input impedance of the stage. The width of the input transistor M_1 is $523\,\mu\mathrm{m}$. Given the size of M_1, the input impedance as seen at the gate of M_1 is predominantly capacitive. To drive this large capacitive load, the input resonator is designed so that it resonates out the capacitive load, thus making it relatively easier to push power in. Since, the resistive parasitics of the L_1 has a significant impact on the Q factor of the resonator, by taking the signal out from the center tap of the L_1, the sensitivity to the resistive parasitics is reduced to a large extent.

The cascode stage is powered by a $1\,\mathrm{V}$ power supply. Biasing for the transistors M_1 and M_2 is achieved by using a resistor tree. In order to provide variability in the bias, transistor M_5 along with a variable current source is used. The transistors are biased to operate in the linear region. As the cascode stage is a scaled down version of the four stack stage, reasoning related to dimensioning of the transistors and capacitors are discussed in Section II-B.

B. Stacked PA

The main PA stage of the design consists of a stack of four transistors. The schematic of the design is shown in Fig. 2. Its structure is essentially similar to the preceding cascode stage with one major difference being in the operating voltage. Similar to the cascode stage, signal is fed via an input resonator, details of which are discussed in Section II-A. As the technology used in this work is a SOI technology, the bulk of the transistors is not connected to the substrate, but, to the source of the device, which in turn is connected to the drain of the lower device. This enables a larger $2.6\,\mathrm{V}$ VDD to be used, which allows increasing the signal swing by a factor of four to $4.4\,\mathrm{V}$ peak-to-peak. As a result, the theoretical maximum output power that can be delivered to a $50\,\Omega$ load is around $17\,\mathrm{dBm}$. Here, $1.1\,\mathrm{V}$ is the permitted VDD for optimal reliability, as specified by the technology design manual.

The gates of the transistors in the stacked structure are not RF grounded but the gate impedances are dimensioned

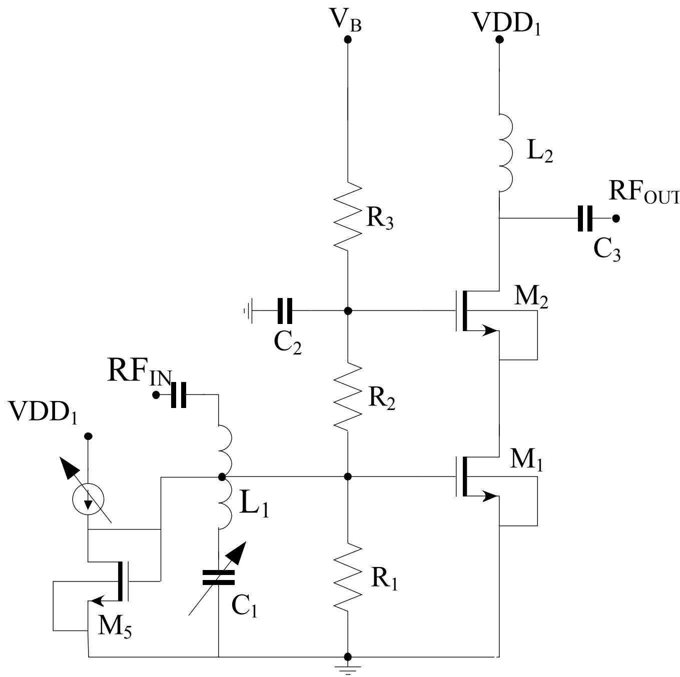

Fig. 1. Schematic of the cascode driver stage.

to control the inter-stage matching and voltage swing in the source nodes of M_2–M_4. Keeping the source waveforms synchronous and progressively increasing is essential in terms of avoiding breakdown. Here, the gate capacitors are optimized to provide minimum delay and linear increase in the voltage swing within the transistors in the stack. In addition, device size and gate capacitances are optimized for direct $50\,\Omega$ load, which relinquishes the need for additional impedance matching, thus simplifying the implementation and minimizing the parasitics and losses. The value of the DC feed coil L_2 along with the coupling capacitor C_5 is jointly optimized to maximize the Q value, which in turn maximizes the gain. The magnitude of the gate capacitances required decreases as one moves up the stack i.e, C_2 is the biggest capacitance at $600\,\text{fF}$ and C_4 is the smallest capacitance at $160\,\text{fF}$. The PA is biased via a resistor tree, providing $450\,\text{mV}$ gate-to-source drive to each transistor, thus, biasing the PA in a moderate class AB region. Similar to the cascode stage, a variable current source along with a diode connected transistor is used to provide a reasonable variability in bias to M_1. Transistors M_1 to M_4 have the same width of $523\,\mu\text{m}$.

There are two main reasons for using the four stack structure. The first reason is related to the input impedance of the structure. The output impedance of the stacked PA is closely dependent on the ON resistance of the complete stack. The output impedance can be tuned by first sizing the transistors in the stack, followed by tuning the gate capacitors. When the number of devices in a stack increases, the size of the individual devices needs be increased too, in order to keep the total ON resistance constant. However, at the same time, the input impedance of the structure reduces as the individual device size is increased. In the current dimensioning scheme, the input impedance goes below $10\,\Omega$ when more than four transistors are stacked. Hence, without an on-chip matching network between the cascode stage and the stacked PA stage, it

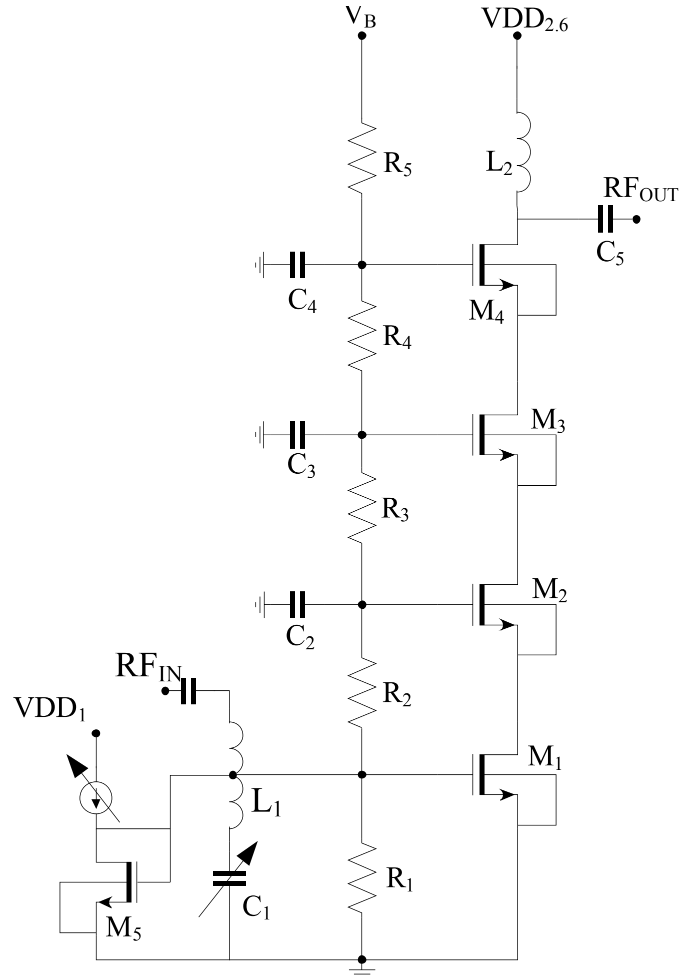

Fig. 2. Schematic of the stacked PA.

becomes difficult to transfer the signal from the previous stage due to the impedance mismatch. Second reason for choosing a four transistor stack is related to the alignment of the swings. As the number of transistors in a stack increases, the phase mismatch between the output of each transistor in the stack increases. Due to this misalignment in the phase, the signal power does not increase proportionally with the increasing number of devices in the stack and thus an additional phase correction mechanism becomes essential. With a four stack structure, it is already difficult to align the swings and the efficacy of the gate capacitors in phase alignment is limited.

III. Experimental Results

The micrograph of the developed integrated circuit (IC) is shown in Fig. 3. The active area occupied by the PA excluding the bondpads is $0.2\,\text{mm}^2$. The active area is circled by a black rectangle in the Fig. 3. The dimensions of the PA, including the input and output pads is $1.0\,\text{mm} \times 0.7\,\text{mm}$. Depending upon the input signal power, the total DC power consumed by the PA varies from $193\,\text{mW}$ to $233\,\text{mW}$. The developed IC is flipped and bonded directly onto the printed circuit board (PCB) via solder bumps. The four layer PCB was manufactured using Isola Astra MT77.

Through, reflect and line (TRL) calibration standards are

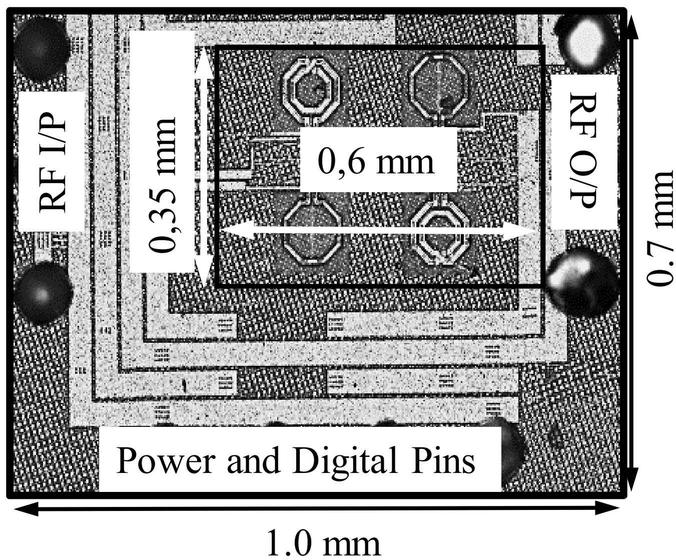

Fig. 3. Chip photograph of the fabricated PA.

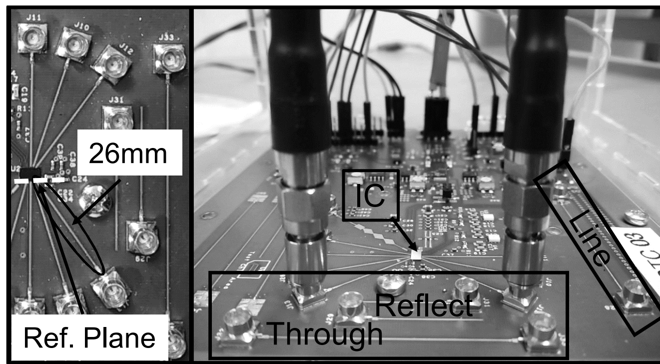

Fig. 4. Photograph of the fabricated PCB.

manufactured on the PCB in order to provide the calibration plane at the edge of the chip. Unfortunately, the manufactured PCB along with the selected SMP connectors and the available mechanical support structures, is not rigid enough to keep the calibration environment and the measuring environment exactly the same. So instead of using a complete two port error calibration based on TRL standards, only normalization calibration based on the through standard was used for the measurements. As a result, only S21 and S12 can be measured reliably and measurements related to S11 and S22 are not included here. Fig. 4 shows the constructed PCB with the chip and the calibration reference plane for measuring the S21. The calibration plane is at the end of the RF feed line and does not include the solder bumps. Hence, the measured results include the additional losses and mismatch caused by the ESD diodes and the pad parasitics, which are roughly in the order of $125\,\mathrm{fF}$ and $70\,\mathrm{pH}$, respectively. The RF feeds are matched to $50\,\Omega$ at RF connector using connectors' 3D simulated model. To accurately measure the power, power calibration is also done using a power meter.

The gain achieved by the PA is shown in Fig. 5. The solid blue color curve in the figure indicates the frequency response at a digital configuration corresponding to the maximum

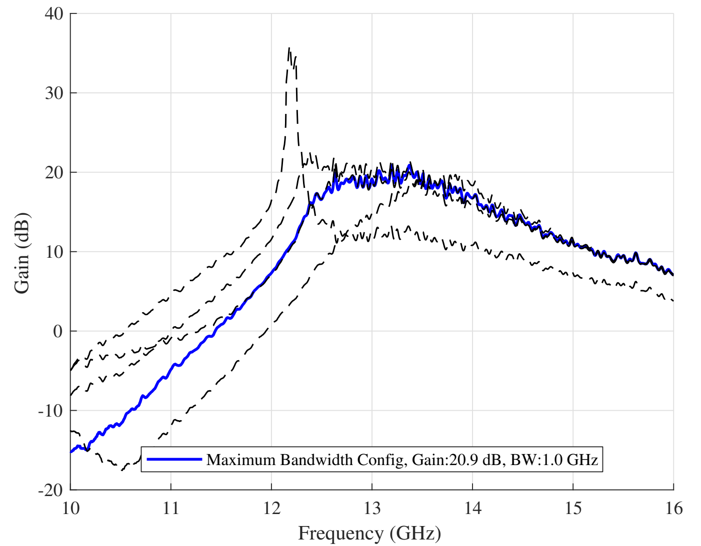

Fig. 5. Gain measured over different digital configurations.

achievable bandwidth. The four dashed black curves indicate the frequency response when the two available resonance controls (one in cascode and one in the stacked PA) are tuned in to their extreme values. It can also be seen from the Fig. 5 that the maximum possible gain of $35.4\,\mathrm{dB}$ is achieved over a narrow bandwidth of $100\,\mathrm{MHz}$ and happens when the resonance frequencies of the two stages align. It can also be seen from the solid blue curve that there is a marginal tilt in the frequency response i.e., gain is marginally higher at the higher end of the frequency band.

The power sweeps for the wide-band digital configuration is shown in Fig. 6. The power sweeps are performed over both edges and at the center of the frequency range. As mentioned earlier, it is clearly visible that the PA can generate larger power at the higher end of the band. The maximum saturated power that the PA can generate is $17.7\,\mathrm{dBm}$ and the DC power consumed at that point is $233\,\mathrm{mW}$. Furthermore, PAE at the band edge is approximately $10\,\%$ higher compared to PAE at the lower frequency edge.

Output 1 dB compression point and peak PAE as a function of frequency is plotted in Fig. 7. Both curves display a clear upward pointing trend, however, the curves are not smooth and the likely reason for this behavior is lack of complete two port calibration. It can be seen from the figure that the peak output 1 dB compression point is $12.3\,\mathrm{dBm}$ and the peak PAE is $23.2\,\%$. The DC power consumed at the peak 1 dB compression point is $200\,\mathrm{mW}$.

A summary of the key performance parameters is shown in Table I. It can be seen from the Table I that given the DC power consumption, the achieved results are competently placed. Higher PAE values are achieved in [4], which also uses a four stack structure. However, it is accomplished by almost doubling the voltage across the drain-source junction in the stacked PA, which unfortunately reduces the reliability of the transistors.

TABLE I. SUMMARY OF THE PERFORMANCE PARAMETERS.

	This work	[4]	[5]	[6]	[7]
Technology	45 nm CMOS SOI	45 nm CMOS SOI	45 nm CMOS SOI	45 nm CMOS SOI	45 nm CMOS SOI
Frequency (GHz)	12–14	12.7–15.3	10–35	4–50	6–26
P_{1dB} (dBm)	12.3 @ 13.7 GHz	-	24.5 @ 18 GHz	-	22.5 @ 18 GHz
P_{sat} (dBm)	17.7 @ 13.7 GHz	25.1 @ 13.5 GHz	27.0 @ 18 GHz	22.5 @ < 20 GHz	26.1 @ 18 GHz
Peak PAE(%)	23.2 @ 13.7 GHz	32.4 @ 13.5 GHz	11.8 @ 18 GHz	24.2 @ 15 GHz	11.0 @ 18 GHz
P_{dc} at P_{sat} (mW)	233.0 @ 13.7 GHz	889.0[a]	1923.0[a]	730.0 @ 10 GHz	-
VDD (V)	1.0 & 2.6	2.0 & 5.0	9.6	1.1 & 6.6	7.2
Stack size[c]	4	4	8	6[d]	6
Active area (mm^2)	0.2	1.0[b]	0.34[b]	0.28	0.16

[a] calculated from drain efficiency.
[b] including pads.
[c] final stage.
[d] in one branch.

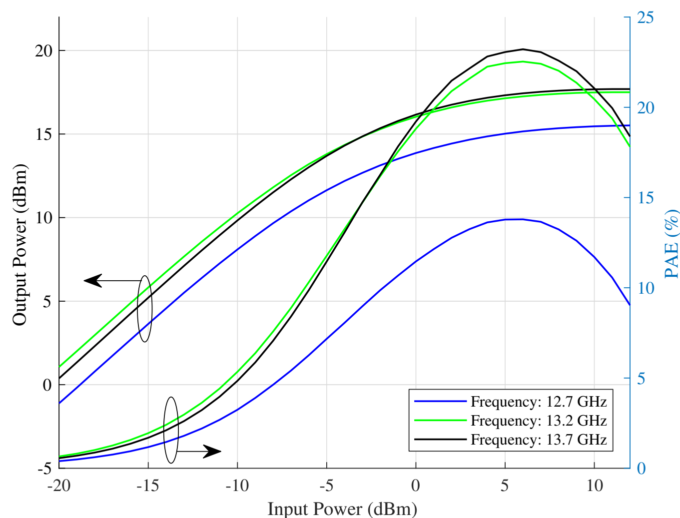

Fig. 6. Output power and PAE as a function of input power.

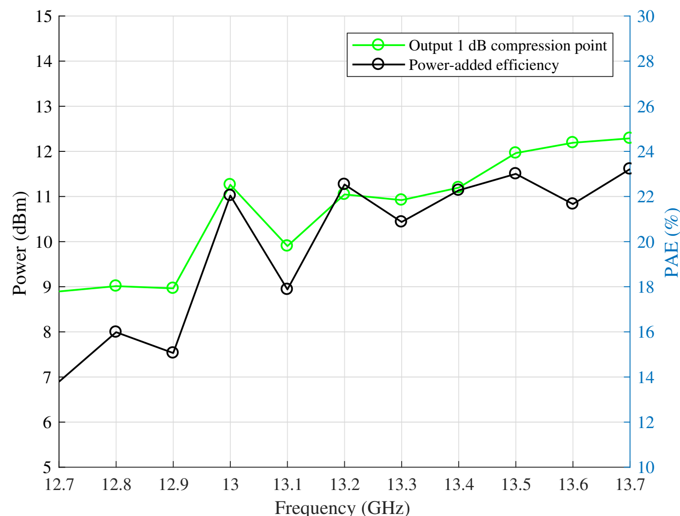

Fig. 7. Output 1 dB compression point and peak PAE as a function of frequency.

IV. CONCLUSION

In this work we demonstrated a package-less fully integrated four stack power amplifier targeted toward 5G communication systems. It was shown that the PA can operate over a frequency range of 12 GHz–14 GHz. The gain and bandwidth of the PA is digitally controllable. Response and receiver power calibration was applied in order to set the reference plane of the measurements at the edge of the IC. In the maximum bandwidth configuration, the PA achieved a maximum saturated power of 17.7 dBm along with a maximum peak PAE of 23.2 % and the output 1 dB compression point of 12.3 dBm. DC power consumed at 1 dB compression point and at saturated output power levels were 200 mW and 233 mW, respectively.

ACKNOWLEDGMENT

The research leading to these results has received funding from the Nokia Corporation Ltd. The authors would also like to acknowledge Global Foundries for the silicon processing and technical support. Support provided by Ganesh Venkatraman, Nuutti Tervo, Risto Vuohtoniemi and Saila Tammelin is highly appreciated.

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