

# A 10-bit Active RF Phase Shifter for 5G Wireless Systems

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**Abstract**—This paper presents an active RF phase shifter with 10 bit control word targeted toward the upcoming 5G wireless systems. The circuit is designed and fabricated using 45 nm CMOS SOI technology. An IQ vector modulator (IQVM) topology is used which provides both amplitude and phase control. The design is programmable with exhaustive digital controls available for parameters like bias voltage, resonance frequency, and gain. The frequency of operation is tunable from 12.5 GHz to 15.7 GHz. The mean angular separation between phase points is 1.5 degree at optimum amplitude levels. The rms phase error over the operating band is as low as 0.8 degree. Active area occupied is 0.18 square millimeter. The total DC power consumed from 1 V supply is 75 mW.

**Keywords**—CMOS, SOI, beamforming, RF, phase shifting, phased arrays, wireless communications, 5G, IQVM.

## I. INTRODUCTION

The expectations of achievable data rates in 5G are approximately a 1000 fold higher compared to current 4G data traffic standard. To achieve these higher data rates, wide band systems operating at centimeter or millimeter wave (mmWave) frequencies are required [1]. Substantial path loss along with the difficulty of RF power generation at these frequencies necessitates using phased array systems with beam steering capabilities [2]. In addition to very high data rates for individual connections, fifth generation wireless systems also target extremely high traffic density. Therefore, sidelobe level reduction to minimize out-of-beam interference is essential. To achieve that, 10 dB of RF amplitude control range will be typically required.

In this paper, we describe an active RF phase shifter targeted towards 5G communication systems. The phase shift is achieved using an IQ vector modulator (IQVM) topology. The design is capable of operating from 12.5 GHz to 15.7 GHz, which is appropriate for prototyping although recent interests in 5G are at 28 GHz, or above. The 10 bit control word encodes both phase and amplitude information and provides 10 dB of RF amplitude control, which is required for amplitude tapering applications.

The organization of the paper is as follows, in Section II, architecture and circuit design for all the related blocks is described, followed by the measurement results in Section III. Conclusions are drawn in Section IV.

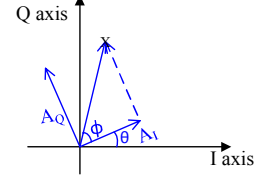


Fig. 1. Principle of operation of an IQVM.

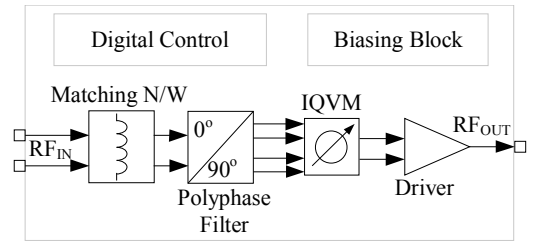


Fig. 2. Block diagram of the developed system.

## II. CIRCUIT DESIGN

The IQVM operates by vector summing of two basis vectors as shown in Fig. 1. Here,  $A_I$  and  $A_Q$  are the rotated I and Q basis vectors with  $\theta$  being the initial phase and  $\phi$  being the generated rotation. Depending upon the sign of the basis vectors, the quadrant of the phase shift according to the following equation

$$\angle \text{RF}_{\text{out}} = \angle \text{RF}_{\text{in}} + \begin{cases} 0^\circ + \arctan \frac{|A_Q|}{|A_I|} & A_Q \geq 0, A_I \geq 0 \\ 180^\circ - \arctan \frac{|A_Q|}{|A_I|} & A_Q \geq 0, A_I \leq 0 \\ 180^\circ + \arctan \frac{|A_Q|}{|A_I|} & A_Q \leq 0, A_I \leq 0 \\ 360^\circ - \arctan \frac{|A_Q|}{|A_I|} & A_Q \leq 0, A_I \geq 0. \end{cases}$$

There are multiple techniques to generate the basis vectors from the original RF signal, for example, polyphase filter, branch line couplers, hybrid couplers, etc., to name a few [3], [4].

A block diagram of the designed system is shown in Fig. 2. The input to the system is a differential signal and the output is single ended. The input is matched to  $100 \Omega$  via the matching network (first block in Fig. 2). After the matching, the differential signal is fed to a polyphase filter which generates differential I and Q signals. These I and Q signals are then combined in the IQVM and a differential signal is generated with the desired phase rotation. This differential signal is then fed to a driver stage which amplifies, converts the signal to single ended and provides a match to  $50 \Omega$ .

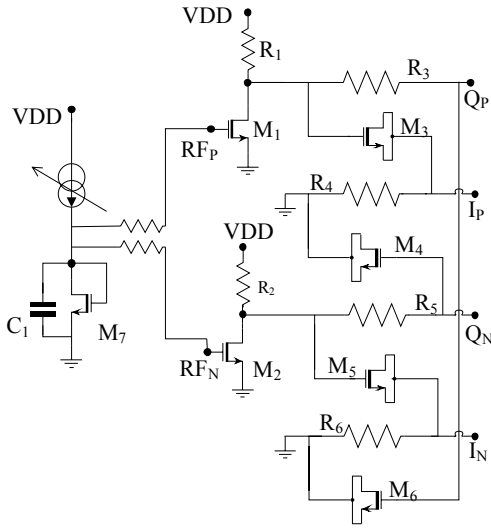


Fig. 3. Polyphase filter with a variable digitally controlled DC biasing.

### A. Polyphase Filter

Polyphase filter can be understood as a combination of low pass and high pass filter [3]. The manner in which the input signal is fed to the polyphase filter, it can be classified into two types; Type-I which has a constant phase difference and Type-II which has a constant amplitude [5]. Here, a constant phase topology is used. Instead of using the traditional interdigitated metal finger capacitors, MOS transistors are used as a capacitive element due to the fact that they are easy to control via digital logic. Furthermore, small capacitance values can be realized more accurately with lower parasitic capacitance.

The complete structure of the implemented polyphase filter is shown in Fig. 3. Transistor  $M_1$  and  $M_2$  are used in a common source topology and are providing DC bias to  $M_3$ – $M_6$ . The DC bias for  $M_1$  and  $M_2$  is provided by using a variable current source along with a diode connected transistor  $M_7$ . As the bias point of the common source stage can be digitally controlled, this inherently gives a control over the realized capacitance value, thus, by changing the bias, the corner frequency of the polyphase filter can be digitally controlled. To keep the gain loss to a manageable level, a single stage polyphase filter was implemented at the cost of its bandwidth.

### B. IQ vector modulator

At block level, the IQVM consists of two sub blocks, the first one is for dictating the sign of the basis vector and the second block is a voltage controlled current source (VCCS), which performs the vector addition, as shown in Fig. 4. In order to change the sign of a vector, cross connected MOS switches are used. Thus, in total, two bits out of ten are used for selecting the appropriate quadrant. As resistive load is used in the summing node, dimensioning for four bits of binary weighted pseudo differential tree becomes difficult because of the limited available voltage swing. To circumvent it, the least significant bit for both I and Q branch is implemented with a unit element, which bleeds only half of the current from the load resistor, with the other half coming directly from

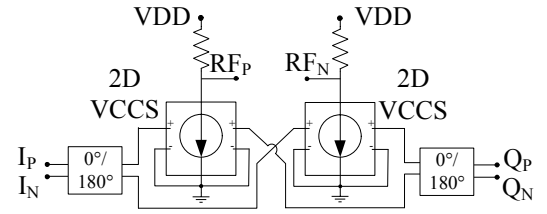


Fig. 4. IQ vector modulator block diagram.

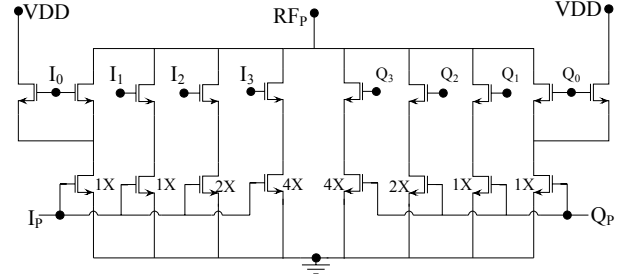


Fig. 5. Positive side of the binary tree used for realizing the VCCS structure used in IQVM. Control bits are numbered from  $I_0$ – $I_3$  and  $Q_0$ – $Q_3$  for I and Q branch respectively.

the supply. Thus, rather than using 1X, 2X, 4X and 8X size elements, 1X, 1X, 2X and 4X size elements are used in the binary weighted tree. The schematic of the positive side of the binary weighted tree is shown in Fig. 5.

### C. Driver

The schematic of the driver stage without the biasing structures is shown in Fig. 6. Transistors  $M_8$  and  $M_9$  along with the variable current source form a differential amplifier. A variable LC tank comprising of a fixed inductor  $L_3$  and a bank of binary weighted capacitors, denoted here by  $C_3$ , is used as a load. The differential output is converted to single ended using a pseudo-differential amplifier consisting of  $M_4$  to  $M_7$ . Transistor  $M_3$  is in a common source topology with a variable resistive load, implemented by connecting digitally controlled MOS in parallel to a fixed resistor. The main purpose of it is to provide a coarse gain control. Finally, the output is taken from a cascode stage consisting of  $M_1$  and  $M_2$ .

The width of the transistors in the driver is gradually increasing, with  $M_8$  being  $18\mu\text{m}$  and  $M_1$  being  $523\mu\text{m}$ . In order to effectively drive such a large device, an input resonator consisting of a fixed inductor  $L_2$  and a variable capacitor  $C_2$  is used. By changing the value of  $C_2$ , frequency response of the stage can be altered. Furthermore, it allows the output DC feed inductor  $L_1$  and coupling capacitor  $C_1$  to be chosen more freely, which are jointly optimized to maximize the Q value in order to maximize the gain. Since, the resistive parasitics of  $L_2$  has a significant impact on the Q factor of the resonator, by taking the signal out from the center tap of the  $L_2$ , the sensitivity to the resistive parasitics is reduced to a large extent.

## III. EXPERIMENTAL RESULTS

The developed active phase shifter integrated circuit (IC) is fabricated using 45 nm CMOS SOI technology and its

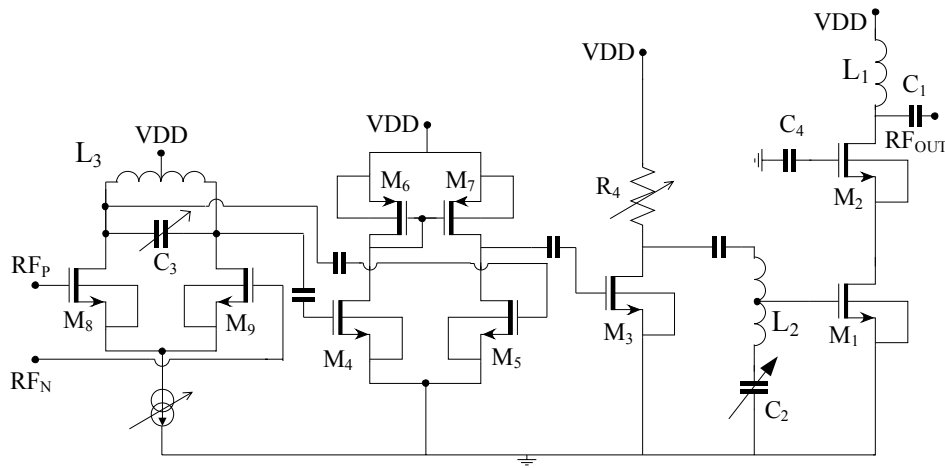


Fig. 6. Simplified schematic of the driver stage.

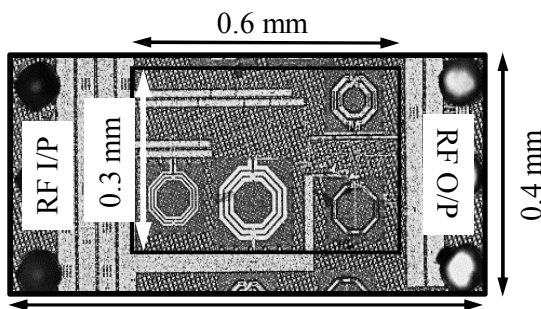


Fig. 7. Chip photograph of the fabricated IQVM.

micrograph is shown in Fig. 7. The dimensions of the IQVM including the input and output pads is  $1.0 \text{ mm} \times 0.4 \text{ mm}$ . The core area of the IQVM is  $0.18 \text{ mm}^2$  and is circled by a black rectangle in Fig. 7. The maximum DC power consumed from 1 V supply by the IQVM is 75 mW. The IC is flipped and bonded directly onto the printed circuit board (PCB) via solder bumps. The four layer PCB was manufactured using Isola Astra MT77.

Vector signal measurements are done using Keysight PNA-X N5247A. Due to the absence of an external absolute phase reference, a fixed digital control word of the IQVM is considered as a reference for all phase measurements. Hence, no calibration is applied to the phase measurements. Since only relative phase and magnitude information is of interest, the lack of calibration is not a hindrance in interpreting the results. All 1024 different phase and amplitude points is shown in Fig. 8. It can be seen from the figure that there is a marginal skew in the measured phase constellation, which implies that the phase difference between the I and Q basis vectors is not  $90^\circ$  but rather close to  $85^\circ$ . Furthermore, it seems that in the fourth quadrant ( $A_I \geq 0, A_Q \leq 0$ , lower right half) the gain is marginally smaller compared to other three quadrants.

It is inherent in the design of an IQVM that there are more number of phase points at higher gain settings compared to lower gain settings i.e., the phase resolution is not independent of the gain. This leads to a case where multiple phase points have similar magnitude and the phase difference between them is less than  $0.5^\circ$  i.e., for all practical purpose they are

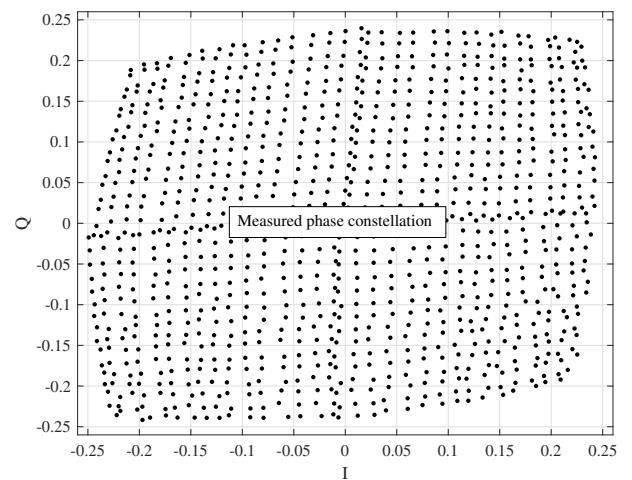


Fig. 8. Measured gain and phase points at 15.0 GHz.

indistinguishable. To quantify this reduction in control space, the number of effective bits is defined as  $\log_2 N_u$ , where  $N_u$  is the total number of unique phase points over the available magnitude range. Here, unique phase points are defined as phase points which have a phase difference of at least  $0.5^\circ$  given the difference in their magnitude is less than 1 dB. The available number of unique phase points as a function of their normalized magnitude is plotted in Fig. 9. It also depicts the mean angular separation as a function of normalized gain. It can be seen from Fig. 9 that the behavior of the IQVM is similar over the operating frequency band. Compared to an idle IQVM, i.e., one which does not suffer from issues like component mismatch, gain mismatch, or compression, the realized IQVM suffers marginally in terms of unique phase points. The rms phase error for a fixed digital configuration of the resonance controls is shown in Fig. 10. It can be seen that the minimum rms error occurs at 15.0 GHz.

The normalized frequency response of the IC for different digital configuration of the resonance controls is shown in Fig. 11. The blue and the black curves illustrate the tuning range of the resonance controls. It can be seen from the figure that the 3 dB tuning range is from 12.5 GHz to 15.7 GHz.

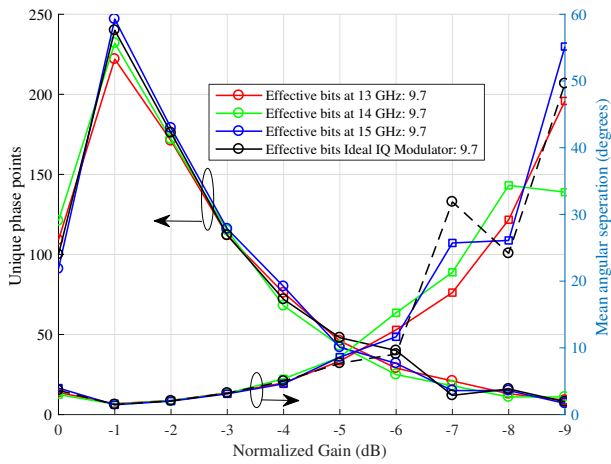


Fig. 9. Number of available unique phase points and angular separation between them at chosen gain values.

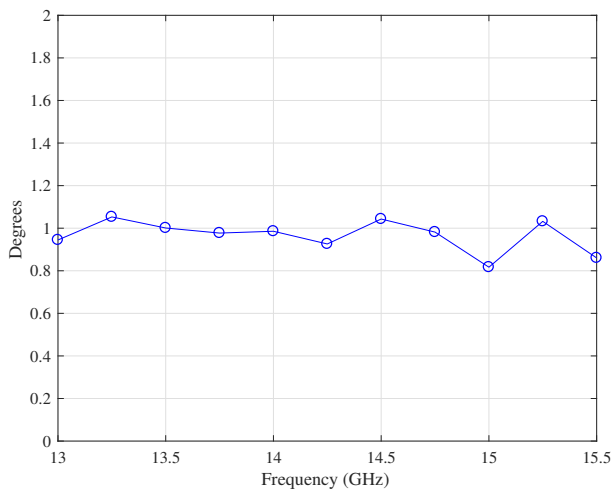


Fig. 10. RMS phase error over the operating frequency band.

Furthermore, the 3 dB bandwidth for a given digital configuration is 2.5 GHz. Finally, a summary of the key performance parameters is shown in Table I.

#### IV. CONCLUSION

In this work we demonstrated a package-less active phase shifter IC targeted toward 5G communication systems. The measured mean angular separation between phase points was  $1.5^\circ$  at optimum amplitude levels. The minimum rms phase error was  $0.8^\circ$  and occurred at 15.0 GHz. The designed phase shifter could operate over a frequency range of 12.5 GHz–15.7 GHz with a RF bandwidth of 2.5 GHz. The DC power consumed was 75 mW.

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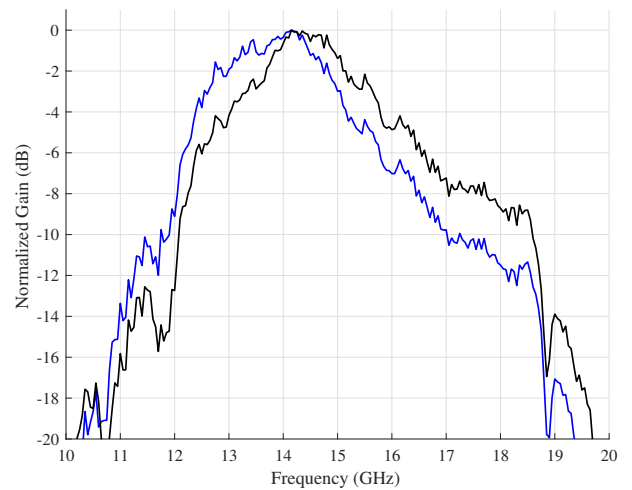


Fig. 11. Frequency response of the fabricated IC at different resonance control configurations.

TABLE I. SUMMARY OF THE PERFORMANCE PARAMETERS.

	This work	[6]	[4]	[7]	[8]
Frequency (GHz)	12.5–15.7	25.0–33.0	78.8–92.8	84–102	60–67
RMS phase err. ( $^\circ$ )	< 1.1	< 5.0	< 11.9	< 12	< 3
Resolution (bits)	10	5	4	4	3
Area ( $\text{mm}^2$ )	0.18	3.3 <sup>a</sup>	0.12	–	–
Total DC Power (mW)	75	0	21.6	–	15
Voltage (V)	1	1	1.2	2	1.3
Topology	IQVM	Passive	IQVM	IQVM	Passive
Technology	45 nm CMOS SOI	45 nm CMOS SOI	28 nm FDSOI	SiGe BiCMOS	45 nm CMOS SOI

<sup>a</sup> Total area of two channels.

#### REFERENCES

- [1] J. G. Andrews *et al.*, “What will 5g be?” *IEEE Journal on selected areas in communications*, vol. 32, no. 6, pp. 1065–1082, 2014.
- [2] W. Roh *et al.*, “Millimeter-wave beamforming as an enabling technology for 5g cellular communications: theoretical feasibility and prototype results,” *IEEE Commun. Mag.*, vol. 52, no. 2, pp. 106–113, Feb. 2014.
- [3] M. J. Gingell, “Polyphase symmetrical network,” US Patent US3 559 042 A, 1971.
- [4] D. Pepe and D. Zito, “Two mm-wave vector modulator active phase shifters with novel IQ generator in 28 nm FDSOI CMOS,” *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 344–356, Feb. 2017.
- [5] J. Kaukoviuri, K. Stadius, J. Ryyanen, and K. A. I. Halonen, “Analysis and design of passive polyphase filters,” *IEEE Trans. Circuits Syst. I*, vol. 55, no. 10, pp. 3023–3037, Nov. 2008.
- [6] U. Kodak and G. M. Rebeiz, “Bi-directional flip-chip 28 GHz phased-array core-chip in 45nm CMOS SOI for high-efficiency high-linearity 5g systems,” in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2017, pp. 61–64.
- [7] F. Golcuk, T. Kanar, and G. M. Rebeiz, “A 90 - 100-GHz 4 x 4 SiGe BiCMOS Polarimetric Transmit/Receive Phased Array With Simultaneous Receive-Beams Capabilities,” *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 8, pp. 3099–3114, Aug. 2013.
- [8] M. Uzunkol and G. M. Rebeiz, “A 65 GHz LNA/phase shifter with 4.3 dB NF using 45 nm CMOS SOI,” *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 10, pp. 530–532, Oct. 2012.