

A 45nm CMOS SOI, Four Element Phased Array Receiver Supporting Two MIMO Channels for 5G

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Abstract—A four element, two channel Multiple-Input Multiple-Output (MIMO) phased array receiver at 15 GHz is designed and fabricated in 45nm CMOS SOI process. The receiver consists of two independent four-antenna phased-arrays for hybrid beamforming and MIMO processing in digital domain. Phase and amplitude control is based on RF IQ vector modulator (VM) at carrier frequency. Measured downconversion gain and noise figure (NF) of one path are 23 dB and 5.4dB, respectively, giving estimated 3.4 dB NF for the IC when simulated PCB and matching losses are taken into account. 1 dB compression and IIP3 points are -37 dBm and -28 dBm, respectively. One phased array consumes 486 mW DC power from 1.2V power supply. Total chip area is 5.69 mm².

Keywords—CMOS SOI, RF, mmWave, beamforming, receiver, phased array, vector modulator, wireless communication, 5G

I. INTRODUCTION

To cope with higher data rates demand for future wireless devices and services, requirements of broader bandwidth and signal to noise ratio (SNR) of radio links have increased [1]. Bandwidth of a few hundred MHz is not available in currently used frequency bands, which leads us to unused bands available in millimeter wave or centimeter wave frequencies. Due to the inherent features of antenna beam-steering and providing improvements in SNR, receiver phased array systems are emerging as strong candidates for fifth generation (5G) communication systems [2]. Phased arrays and beamforming (BF) techniques have been a central factor for radar applications [3]. Various phased array architectures at cm-wave and mm-wave frequencies have been reported in literature [2] [3] [4]. RF path phase shifting and combining technique has the advantage of less complexity and lower power consumption, therefore, becoming a typical choice for implementation of CMOS receiver phased arrays.

A communication model and link budget analysis for a future wireless system is proposed in [1]. It has been shown that a minimum SNR of 33 dB is required for implementing higher order modulation schemes such as 256 QAM to achieve maximum non-coded data rate of more than 3 Gbits/s at 500 MHz bandwidth in a communication link. However, 64-QAM with some coding scheme is likely more realistic with link SNR requirement of ~25 dB. In such conditions, a 4-5Gbps data rate requires at least two MIMO channels with independent signal

paths. In addition to capacity, future 5G networks are expected to provide traffic density and spectral efficiency far beyond current radio systems. Therefore spatial filtering and side-lobe reduction are essential design criteria and necessitates amplitude control in addition to phase. Vector modulator, proposed at lower carrier frequencies [5] provides efficient means to control both phase and amplitude thus allowing calibration that can be managed both at the same time.

This paper describes a two-channel RF phased-array receiver implemented in 45nm CMOS SOI process. In Section II, the design topology and key circuit parameters are explained. Measurement results and performance parameter tables are presented in section III. Section IV and V include chip measurements and conclusions, respectively.

II. ARCHITECTURE AND CIRCUIT DESIGN

The proposed receiver consists of two identical phased-arrays for digital MIMO processing. Each phased-array supports four individual antenna elements with phase shifting and combines the received signals in the RF domain. Block diagram of the designed system is shown in Fig 1. Each RF element is comprised of low noise amplifier (LNA), single-ended-to-differential converter (S2D) and IQ vector modulator for phase shifting and amplitude tapering. Two-stage signal combining provides buffering to avoid loading between paths before the RF signal is downconverted to baseband (BB) using a Gilbert cell mixer. An external local oscillator (LO) signal is used which is divided by 2 locally to provide 15 GHz LO signal for IQ downconversion. Digital control provides extensive means to control different gain settings, bias control, RF response tuning, phase, etc.

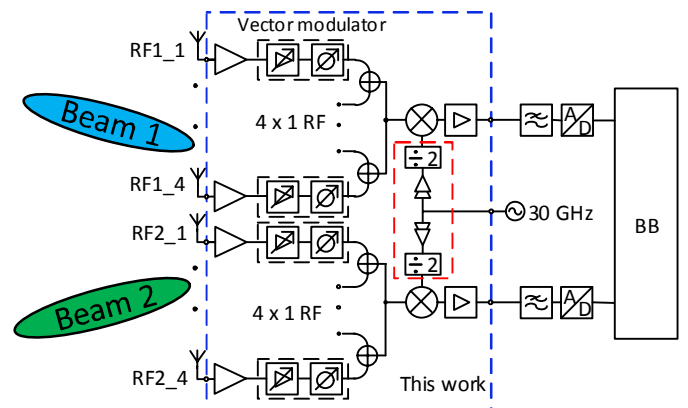


Fig 1: System Block Diagram

A. Low Noise Amplifier

Common-source cascoded inductively degenerated source topology is utilized for LNA design, shown in Fig 2, because of its built-in filtering and matching conditions [6]. Parasitic capacitances from electrostatic discharge (ESD) diodes and input pads with small parasitic inductance from chip internal wiring and solder bump introduce additional reactance at the input. This leads to relatively high Q impedance seen by 50 Ohm source port. Instead of implementing gate inductance on-chip, external matching circuit is implemented with the help of transmission lines. In case of very strong signal the LNA can be bypassed using a switch. A resonance tuning control is realized with PMOS switches, which turn off/on unit capacitance to output load, changing the resonance of the load.

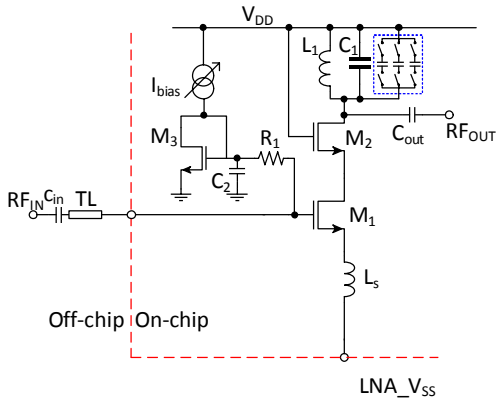


Fig 2 Common-source cascoded low noise amplifier

B. Single-ended to Differential Converter

Active balun circuit for low frequencies has been reported e.g. in [7]. Parasitic components appearing at critical nodes makes the design more challenging at 15 GHz, with minimum phase and gain errors in the output signal. In this work, a gain-boosting current-balancing balun circuit topology [7] is selected as a baseline for single to differential signal converter as shown in Fig 3.

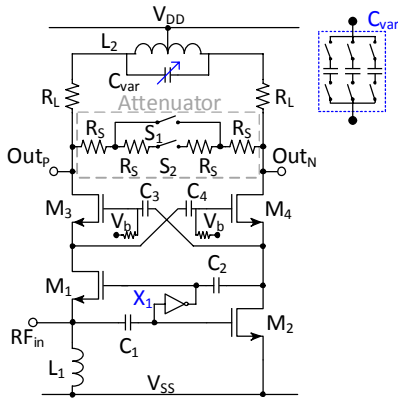


Fig 3: Single-ended to differential converter

S2D circuit is composed of two stages: common gate-common source (CG-CS) M1-M2 input stage for gain boosting and the output current is then balanced by CG devices M3 and M4 with cross coupled input also called differential current

balancer (DCB). All the devices M1-M4 are of equal sizes, i.e. 12um/56nm. A resistive feedback inverter amplifier (X_1) is used to self-bias M1 and M2. A two-step resistive attenuator is implemented at the output. A center-tapped coil is used as a load and for tuning the frequency response at 15 GHz. Resonance tuning is also implemented in this block.

C. IQ Vector Modulator Phase Shifter

RF phase shifter (PS) is the core block of RF phased arrays. Passive structures such as reflection-type PS and switched-line PS are demonstrated in [2] and [4], respectively. Passive phase shifters are very accurate in terms of phase error but area can be large and loss is unavoidable. Vector modulator (VM) phase shifter provides compact size, better noise performance and opportunity to tradeoff with linearity using appropriate gain partitioning in internal amplifiers.

Active digitally controlled 10-bit vector-sum phase shifter topology is used in this work, which provides in total 1024 points in phasor plot in all four quadrants. Block diagram of the phase shifter is shown in Fig 4. A differential signal is split into four quadrature signals with the help of passive poly-phase filter. Each quadrature differential signal is then weighted individually with the help of a Variable Gain Amplifier (VGA), and the output currents from I and Q branches are summed up to form a resultant vector with particular phase. A quadrature selector is used for switching the quadrants of the resultant vector to implement full 360°.

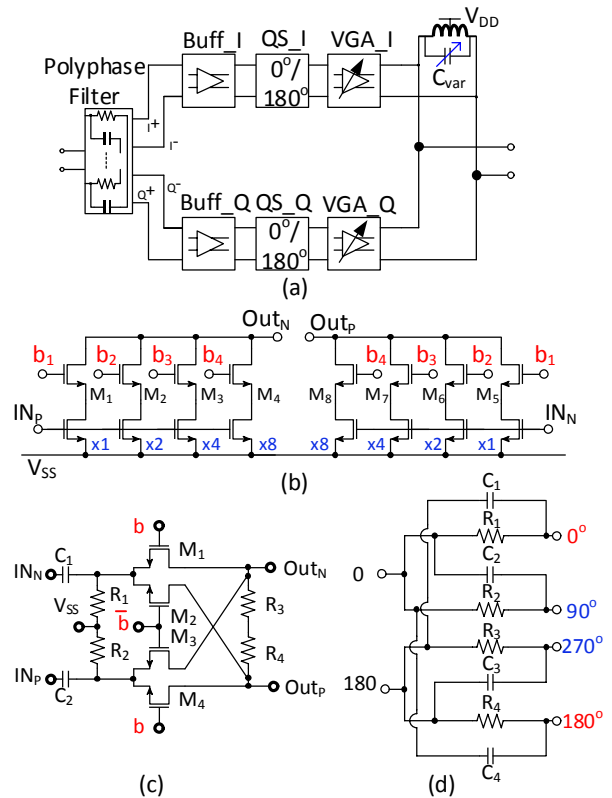


Fig 4: (a) Vector modulator architecture, (b) Variable gain amplifier (c) Quadrature selector (QS), (d) RC Polyphase filter

1) Poly Phase Filter

An RC poly-phase filter topology, shown in Fig 4 (d), is utilized for quadrature generation due to its compact area. To achieve balanced signal at the output careful symmetrical layout is implemented.

2) Quadrature Selector

Quadrature selector block makes the operation of IQ vector possible, in all four quadrants. Circuit diagram of vector selector is shown in Fig 4 (c). NMOS devices are used as switches and can be cross-coupled (reverse) with 1-bit control.

3) Variable Gain Amplifier

Fig 4 (b) shows the schematic of a differential variable gain amplifier (VGA). Common-source NMOS transistors are used as inputs with cascode connection of NMOS switches to digitally control RF current of binary weighted devices. Center-tapped coil with resonance control is for summing the internal signal paths of the vector modulator at the output.

D. Antenna Signal Path Combining

Depending on the used frequency and size of an array, either active (current combining) or passive signal combiners can be used. In large phased array systems, architecture affects gain budget and thus linearity and NF of the whole receiver. Wilkinson power combiners were utilized in [3], while a combination of a passive and active combiners were demonstrated in [4] for 16 elements.

Due to compact size at 15GHz operation a two-stage current combining is implemented in this work using first a parallel differential pair with fixed tail current topology, which provides sufficient isolation from the other paths to avoid loading effects. In the second stage, output currents of the active combiners are summed using a narrowband LC load with low ohmic metal wires. A center-tapped coil is used for supplying DC power to these two combiners and resonate out the wiring capacitances at center node.

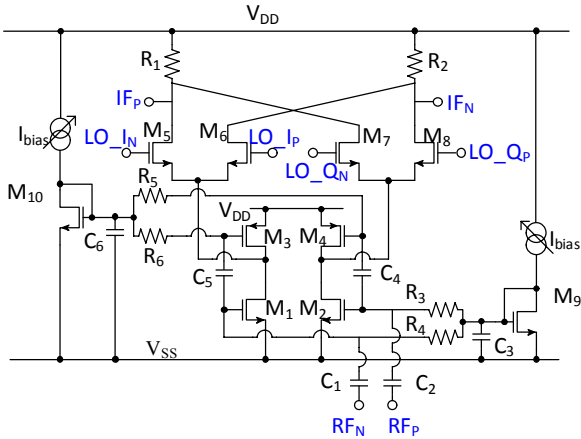


Fig 5: Downconversion Mixer

E. Mixer and IF Amplifier

Mixer schematic is shown in Fig 5. A Gilbert cell type double balanced current reuse topology [8] is used for two mixers, i.e. for I and Q outputs. Mixer input part is composed of a NMOS and PMOS pair connected in cascode, biased

separately from bias blocks. Input RF signal is AC coupled from previous stage and both input devices are also AC coupled from each other. Conventional divide-by-two approach is used to generate I/Q signal from externally generated 30GHz LO signal.

Differential amplifier with resistive feedback is used for buffering the output at baseband. Longer channel length of the output devices is possible due to limited BW up to few hundreds of MHz. The pull up coils of the baseband amplifier are placed off-chip.

III. EXPERIMENTAL RESULTS

Fig 6 shows the micrograph of manufactured chip and the core area is $3.95 \times 1.44 \text{ mm}^2$ including pads. IC is flip-chipped directly on the PCB using solder bumps to minimize parasitics. The designed RFIC has eight RX inputs placed next to each other on the same edge of the IC. In an unpackaged flip-chip, the chip pad areas dictate the pitch of the PCB as well. IO pad pitch is $190 \mu\text{m}$ with the pad area of $80 \mu\text{m} \times 80 \mu\text{m}$. Due to PCB manufacturing limitations, a maximum width of $100 \mu\text{m}$ wide transmission line can be used to feed the signal lines to the input of the LNA near the chip and afterwards can be tapered to wider widths. The four-layer PCB by Isola Astra MT77 was used with the material characteristics of $\epsilon_r = 2.99$ and $\text{loss}(\tan\delta) = 0.0017$. The total thickness of top layer of PCB is 0.09 mm resulting in the linewidth of $230 \mu\text{m}$ (50Ω) using the top metal. Impedance matching of a single receiver at centre frequency of 15 GHz is designed to achieve $S_{11} < -10 \text{ dB}$.

Conversion gain measurements were performed using a vector network analyzer (VNA) using frequency converter option. Cold source method [9] using spectrum analyzer is used for measuring noise figure (NF) of a single RX chain while other chains are switched-off. A single RX element provides a maximum conversion gain of 23 dB at 14.9 GHz , which is 2 dB less than estimated in post-layout simulations. Single chain RF response and S_{11} curves are shown in Fig 7, while other branches are terminated to 50Ω . Two-tone test for IIP3 measurement is performed at 20 MHz frequency offset and extrapolated curve gives $\text{IIP3} = -28 \text{ dBm}$ (see Fig 8). Measured noise figure (NF) for a single channel at 14.9 GHz is 5.4 dB without PCB losses. Simulated PCB loss is 2 dB that corresponds to NF of 3.4 dB in the chip, which is within 0.2 dB of simulated value. Measurements of phase shifter constellation points are done with the help of IQ analyzer option of Keysight UXA N9040B and are shown in Fig 9. The RX chain showed some coupling from VM output to LNA input, and the points in Fig 9. are measured with LNA bypass. Measured power consumption of one 4-element receiver phased-array is 463 mW .

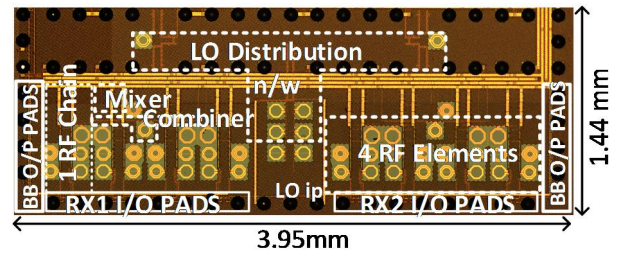


Fig 6: Chip micrograph of a two channel phased array

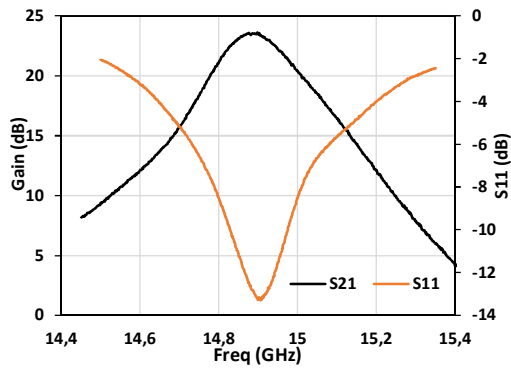


Fig 7: Measured S11 and S21 (Fixed IF=100MHz)

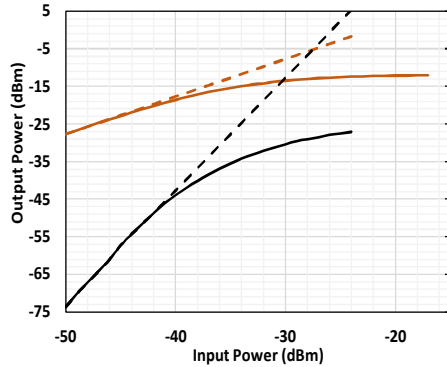


Fig 8: Measured IIP3

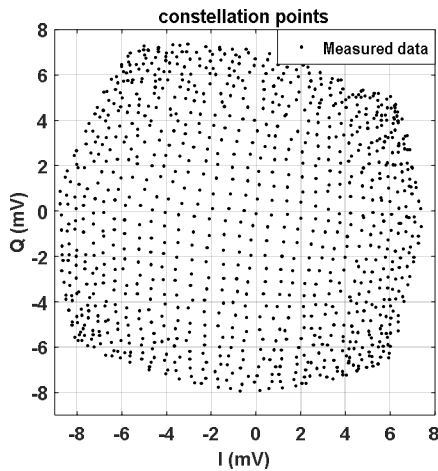


Fig 9: Phase shifter constellation points in all quadrants

IV. CONCLUSIONS

A two MIMO channel four element receiver phased array was demonstrated using 45nm CMOS SOI technology. Phased array chip was fabricated and measured. Measured results from a single element show maximum gain and noise figure of 23 dB and 5.4 dB (3.4 dB without PCB losses), respectively, at 14.9 GHz. The two phased-arrays consumes smallest area than the state of the art designs, mentioned in Table 1. An IQ VM phase shifter was implemented at 15 GHz, which provides opportunity to fine tune the phase and amplitude of signal in each element. In addition to inherent gain controllability of VM,

digital programmability is also implemented in different blocks which results in gain control range from 6 dB to 23 dB.

TABLE I. PERFORMANCE COMPARISON

	<i>This work</i>	[2]	[3]	[4]
Freq (GHz)	15	28	10	60
Array Size	4	32	4	16
Phase Shifter	Active	Passive	Passive	Active
Single path gain (dB)	23	34	10.1	58
NF (dB)	5.4 ^a	3.7	3.4	7.4
1 dB Comp. (dBm)	-37	-22.5	-12.5	-16
IIP3 (dBm)	-28	N/A	-4	N/A
DC Power Consum. (mW)	463 ^b	3300	144	1800 ^c
Area (mm ²)	1.807 ^d	165.3	7.25	37.7 ^c
Technology	45nm CMOS SOI	0.13 μ m SiGe BiCMOS	130nm CMOS	SiGe BiCMOS

^a Including 2 dB estimated PCB losses from chip-PCB interface

^b 4-element phased-array measurement

^c Area and DC power consumption of both TX and RX

^d Area of a 4 element RF phased-array excluding LO distribution network

V. ACKNOWLEDGEMENT

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