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MASTER'S THESIS

LINEARITY ANALYSIS OF A BEAMFORMING PHASED ARRAY RECEIVER

Author	Mahmoud Shehab
Supervisor	Timo Rahkonen
Second Examiner	Janne P. Aikio

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ABSTRACT

This thesis introduces the linearity analysis of the beamforming phased array receiver. The receiver is consisting of many parallel RF and IF modules. The IF module is working at frequency from 2-4 GHz. The analysis in this thesis is mainly concentrated on how we can take advantage of the parallelism to improve the linearity of both the LNA and the passive mixer. This can be achieved by introducing a minor offset in the output operating point of the parallel blocks, so that the 3rd order nonlinearity coefficients would have opposite signs. This would then cause some cancellation of distortion in the combined output. The analysis shows that the GM stage linearity can be improved up to 30 or 50 dB by slight deviations in the biases of neighbouring GM stages. The previous cancellation needs very good matching so 10-15 dB cancellation is probably a realistic to achieve. The linearity of the passive mixer can be further improved by 10 dB. The linearity analysis is made by building up a polynomial model of the block and then study the first, second and third order coefficients.

Some other design parameters for both the GM stage and passive mixer are analysed such as noise figure, input and output impedance.

Key words: Beamforming, Phased array, transconductance LNA amplifier, current mode passive mixer, Taylor series, Volterra series, polynomial.

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FOREWORD

I would like to thank ALLAH for providing me the strength and ability to complete the thesis right on time. I would like to express my special gratitude to Prof. Timo Rahkonen for assisting, directing and guiding me throughout my thesis. His benignant and friendly response let me finish my thesis on time. I would like also to thank Janne P. Aikio for reviewing my thesis.

In addition, I wish to acknowledge the commendable support that I got from my family. Their support throughout my life have given me the strength to believe in myself. I will always be indebted for their lifelong support.

Oulu, May 01, 2020

Mahmoud Shehab.

LIST OF ABBREVIATIONS AND SYMBOLS

MIMO	Multiple Input Multiple Output
BF	Beamforming
RF	Radio frequency
IF	Intermediate frequency
5G,4G	4^{th} and 5^{th} mobile generation
s/p	Serial to parallel conversion
DOA	Direction Of Arrival
ACPR	Adjacent Channel power Ratio
LTE	Long Term Evolution
3GPP	3^{rd} generation partnership project
CMOS	Complementary Metal oxide Semiconductor
SNR	Signal to Noise Ratio
LNA	Low Noise Amplifier
TLNA	Transconductance Low Noise Amplifier
VGA	Variable Gain Amplifier
PGA	Programable Gain Amplifier
DAC	Digital to Analog Converter
LO	Local Oscillator
NF	Noise Figure
GM	Transconductance
IIPn	Nth order Input Intercept Point
I/Q	Inphase and Quadrature components
TIA	Transimpedance Amplifier
BB	Baseband
QAM	Quadrature Amplitude Modulation
λ	Wavelength
f_c	Carrier Frequency
$x_{\mathrm{n}}(t)$	Received signal at the input of the receiver
$\widetilde{x_{\mathrm{n}}}(t)$	Low pass component of the received signal
y(t)	Received signal at the output of the receiver
τ	Time delay
$\theta, \emptyset$	Incident angle of the signal on the receiver
d	distance between the antennas
c	signal velocity in space
$w = A_r + jA_i$	Complex weighting
f_{LO}	Frequency of the Local Oscillator
x_i	Inphase signal component
x_q	Quadrature signal component.
n	Turns ratio of the transformer
L_s, L_p	Primary and secondary inductance
M	Mutual inductance
k	Coupling coefficient
K_n	Coefficients of Taylor series
HDn	nth order Harmonic Distortion
THD	Third order Harmonic Distortion

IMn	nth order intermodulation distortion.
Ids	Total drain to source current
Vgs	Total gate to source voltage
Vds	Total drain to source voltage
Hn	Volterra kernel
$h(\tau)$	Impulse response
rop	Output resistance of PMOS
ron	Output resistance of NMOS
gmn	Transconductance of NMOS
gmp	Transconductance of NMOS
gm'	First derivative of transconductance
gds	On conductance
Wn	Width of the NMOS
Wp	Width of the PMOS
cgd	Gate to drain capacitance
cgs	Gate to source capacitance
K_B	Boltzmann Constant
T	Absolute temperature
S_{11}	Scattering parameter
v_n	Noise voltage

1 INTRODUCTION

The phased array system was developed early between 1930s and 1940s in the applications of the radar at which multiple omni directional antennas with the phase shifters. The aim was to allow the receiver to detect the weak signal and enable the directional finding as well. There are many types of phased array receiver.

Nowadays massive MIMO (multiple Input Multiple Output) and the beamforming (BF) are two essential concepts in the 5^{th} mobile generation. In the 5G communications, the antennas will operate at very high frequency called mm wave frequencies such as 28 GHz. At these frequencies, the wavelength is in a range of few millimeters. These allow many antennas to be placed very close to each other with separation of $\lambda/2$.

MIMO systems contains large number of antennas at the transmitter and the receiver at which different data streams are transmitted from each of the transmit antenna and the receive antenna then receive signal from all the transmit antennas. These large number of antennas provide higher spectral and energy efficiency. There are many types of antennas that can be used for this purpose, for example the smart antennas which are antenna arrays with smart signal processing algorithm used to identify spatial signal signatures such as direction of arrival (DOA) of the signal. This type of antenna can be used both in the base stations and in the user mobile.

Beamforming (BF) is focusing the signal in one direction, where the transmitter is delivering a high-quality signal with high power and less errors with no need to boost the broadcasting power. It uses multiple antennas with a separation of $\lambda/2$. It also provides interference rejection for the adjacent channels, this helps in improving the adjacent power channel ratio (ACPR) which can be defined as the ratio between the adjacent channel power to the main channel power. The overall system performance increases by using both of the previously stated techniques.

There are pros and cons from these techniques , for example, very high data rate (2x2 MIMO system roughly double the data rate of a single antenna with the same bandwidth) and spatial diversity are two of the most essential pros, while the range (coverage area) is a disadvantage. Although MIMO has been around for decades, people does not actually take advantages of it, as the number of the antennas used is small. Nowadays, in the 3GPP release 15, the number of antennas used in the LTE is 64.

In this thesis, the linearity of a certain beamforming receiver is studied. It also studies the possibility of utilization of the parallelism in improving the linearity of the receiver. Finally, the thesis gives some notes on the choice of the bias point to improve the third order intercept point of each part of the receiver. A simulation of the receiver parts with 45nm CMOS technology is also provided, for example, the GM stage, passive mixer and phase switches. the linearity was studied by taking the raw data from cadence and plug it in a MATLAB code that makes the polynomial model and Volterra series for the device and gives plots for dc, first, second, third order coefficients.

This thesis is divided into 5 chapters. Chapter 2 is discussing several implementations of the beamforming receivers, it also includes the wideband scalable receiver which is the one under study in this thesis. Chapter 3 introduces some of the basic linearity concepts and analysis for example Volterra, polynomial and Taylor series. Chapter 4 discusses the GM block design and its linearity analysis while chapter 5 discusses the passive mixer design and its linearity analysis. The circuit analysis in the thesis is unfortunately somewhat scattered, due to tight access permissions. Some data are based on a real implemented prototype, but some are obtained by simulating similar structures in a more easily accessible process.

2 BEAMFORMING RECIEVER ARCHITECTURE

The beamforming receiver generally consists of multiple antennas with a separation of λ/2. The aim is to combine the received signal at different delay times and at different amplitudes so that the desired signal is enhanced and the interfering signal from another direction is cancelled.

This process generally improves the sensitivity of the receiver. Beamforming requires programmable gain and phase shift which can be implemented in various ways.

2.1 Receiver spatial multiplexing

It is important to highlight some of the basic concepts. For example**, spatial Multiplexing**, which is a transmit technique that is used in the 4G and 5G networks. The data stream is divided and transmitted through different independent channels.

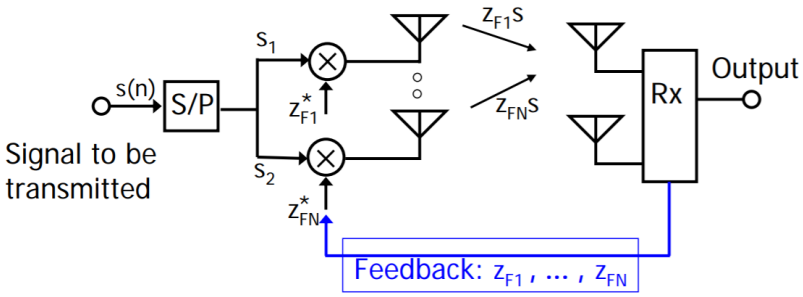

Figure 1: Spatial multiplexing

Space-time equalization is needed in the receiver which results in having the number of the receive antenna greater than the number of the transmit antenna. The receiver can perform channel estimation and provide data back to the transmitter to improve the performance.

In **Receive spatial multiplexing,** multiple antennas in the receiver are used. They are separated such that the fading of each antenna element is uncorrelated, which helps in enhancing the signal quality from the multipath fading environment. Also, complex weighting could be added in each branch which helps in maximizing the SNR and suppressing some of the interfering signal [1].

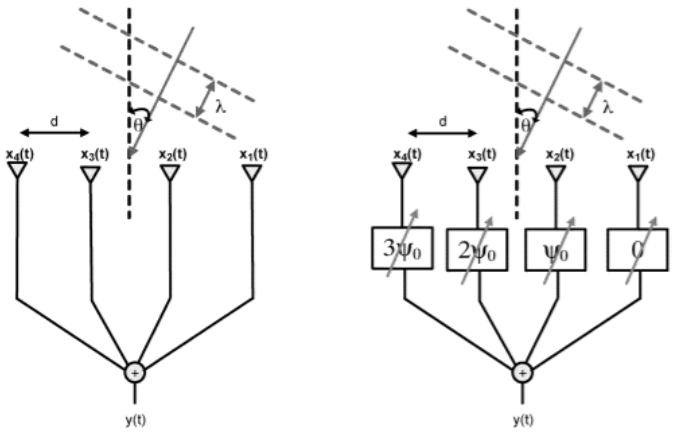

Figure 2: Beamforming simple array and phased array

Imagine having a plane wave that is incident on the phased array receiver. The received signal in each antenna can be given by the following equations [1]

$$x_1(t) = Re\left[\widetilde{x_1}(t)\, e^{j2\pi f_c t}\right] \tag{1}$$

where $x_1(t)$ is the received signal, f_c is the carrier frequency and $\widetilde{x_1}(t)$ is the lowpass component of the transmitted signal.

The received signal is incident with angle θ with respect to the normal. It can be noticed that the signal reaching the second element from the right is delayed from that reached the most right element. This delay can be calculated by the following equation.

$$\tau = \frac{d \sin(\theta)}{c} \tag{2}$$

where d is the separation between each element and c is the signal velocity in the space. So, the signal in the consecutive branches can be expressed as $x_{\mathrm{k}}(t) = x_1(t - k\tau)$. The summed output (received) signal can be expressed by the following equation.

$$y(t) = Re\left[\sum_{k=0}^{N-1} \widetilde{x_1}(t - k\tau)\, e^{j2\pi f_c (t - k\tau)}\right] \approx Re\left[\left\{\sum_{k=0}^{N-1} e^{-j2\pi f_c k\tau}\right\} \widetilde{x_1}(t)\, e^{j2\pi f_c t}\right] \tag{3}$$

As can be noticed from the previous equation an approximation has been done for the low pass component of the transmitted signal. It is assumed to be equal for the delayed signals. The low pass component of the signal can be expressed by the following equation.

$$\tilde{y}(t) = \left\{\sum_{k=0}^{N-1} e^{-j2\pi f_c k\tau}\right\} \widetilde{x_1}(t) = \left\{\sum_{k=0}^{N-1} e^{-jk\Psi}\right\} \widetilde{x_1}(t) \tag{4}$$

where $\Psi = 2\pi f_c \tau$. As can be seen in Figure 2 each of the receive path has a programmable phase shifter with phase shift $\mathrm{k}\Psi_o$. Then finally the low pass signal can be written as in the following equation.

$$\tilde{y}(t) = \left\{\sum_{k=0}^{N-1} e^{-jk(\Psi + \Psi_o)}\right\} \widetilde{x_1}(t) \tag{5}$$

From this equation, we can notice that phase shift $\mathrm{k}\Psi_o$ is used to cancel the phase shift caused by time delay for the signal to travel from one branch to another. The main lobe of the array pattern is rotated to be corresponding to the direction of the received signal which result in coherent detection of the received signal, while there will be nulls and side lobes in the other directions results in suppressing other signals. So, an important information should be known and estimated by the receiver, the direction of arrival of the needed received signal. There are many methods and algorithms to do so for example the music algorithm [24].

One advantage that seems clear from the previous analysis is that the antenna elements are very close to each other, which makes the received signal amplitudes correlated and phase shifted. This results in coherent signal summation. Doubling the number of the antennas will results in 3dB enhancement in the SNR.

A practical example [2] is shown in the next part of how the complex weighting in the branches of the beam forming receiver are going to enhance certain signal and reject another. Let's assume that we have two signals $s_1(t)$ and $s_2(t)$ (two channels). Each of the two signals are incident with different angles $\emptyset_1$ and $\emptyset_2$. We have only two branches in the receiver end with two complex weights $w1$ and $w2$ and the angle of arrival is known a prior.

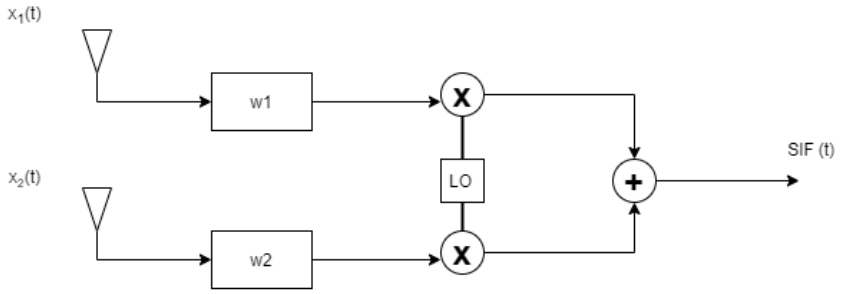

Figure 3: Two antenna array receiver.

Now the complex signal in front of the antenna elements can be given as in the following equations.

$$x_1(t) = \left[\widetilde{s_1}(t)\, e^{j2\pi f_{c1}t} e^{j\pi\frac{d}{\lambda}\sin(\emptyset_1)}\right] + \left[\widetilde{s_2}(t)\, e^{j2\pi f_{c2}t} e^{j\pi\frac{d}{\lambda}\sin(\emptyset_2)}\right] \tag{6}$$

$$x_2(t) = \left[\widetilde{s_1}(t)\, e^{j2\pi f_{c1}t} e^{-j\pi\frac{d}{\lambda}\sin(\emptyset_1)}\right] + \left[\widetilde{s_2}(t)\, e^{j2\pi f_{c2}t} e^{-j\pi\frac{d}{\lambda}\sin(\emptyset_2)}\right] \tag{7}$$

Now the IF signal can be given as in the following equation.

$$\begin{aligned} s_{IF}(t) = \Bigg[& w_1 \left[\widetilde{s_1}(t)\, e^{j\pi\frac{d}{\lambda}\sin(\emptyset_1)} + \widetilde{s_2}(t)\, e^{j\pi\frac{d}{\lambda}\sin(\emptyset_2)} \right] \\ & + w_2 \left[\widetilde{s_1}(t)\, e^{-j\pi\frac{d}{\lambda}\sin(\emptyset_1)} + \widetilde{s_2}(t)\, e^{-j\pi\frac{d}{\lambda}\sin(\emptyset_2)} \right] \Bigg] e^{-j2\pi f_{IF}t} \end{aligned}$$

$$\begin{aligned} s_{IF}(t) = \Bigg[& \widetilde{s_1}(t) \left[w_1\, e^{j\pi\frac{d}{\lambda}\sin(\emptyset_1)} + w_2\, e^{-j\pi\frac{d}{\lambda}\sin(\emptyset_1)} \right] \\ & + \widetilde{s_2}(t) \left[w_1\, e^{j\pi\frac{d}{\lambda}\sin(\emptyset_2)} + w_2\, e^{-j\pi\frac{d}{\lambda}\sin(\emptyset_2)} \right] \Bigg] e^{-j2\pi f_{IF}t} \end{aligned} \tag{8}$$

Consequently, if we want to detect $s_1(t)$ and supress $s_2(t)$, the following two equations needed to be fulfilled.

$$\left[w_1\, e^{j\pi\frac{d}{\lambda}\sin(\emptyset_1)} + w_2\, e^{-j\pi\frac{d}{\lambda}\sin(\emptyset_1)} \right] = 1 \tag{9}$$

$$\left[w_1\, e^{j\pi\frac{d}{\lambda}\sin(\emptyset_2)} + w_2\, e^{-j\pi\frac{d}{\lambda}\sin(\emptyset_2)} \right] = 0 \tag{10}$$

By solving these two equations and determining w_1 and w_2 which are the complex weighting we can easily suppress the unwanted signal.

2.2 Cartesian combining receiver

Programmable RF phase shifters are lossy and difficult to make. A clever way of implementing a beamforming using Cartesian combining is presented in [2]. Let us explain its structure by starting from a traditional two antenna receiver shown in Figure 4.

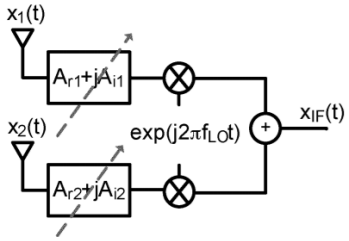

Figure 4: Complex weighting and down conversion [2].

The idea is to have a 90° phase shift in the form of complex down conversion. Since the multiplication and the addition are commutative the receiver could be as shown in Figure 5

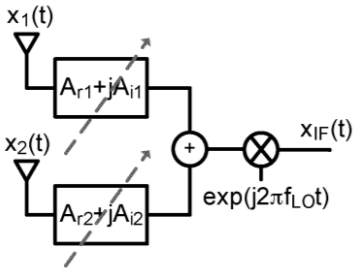

Figure 5: Commutative property [2]

So, the IF signal can be represented according to the following equations

$$x_{if}(t) = (A_r + jA_i)e^{j\,2\pi f_{lo}t} \tag{11}$$

$$xi(t) = x(t)[A_r \cos(2\pi f_{lo}t) - A_i \sin(2\pi f_{lo}t)] \tag{12}$$

$$xq(t) = x(t)[A_i \cos(2\pi f_{lo}t) + A_r \sin(2\pi f_{lo}t)] \tag{13}$$

From equations (12,13), we can conclude that the receiver can be as shown in Figure 6.

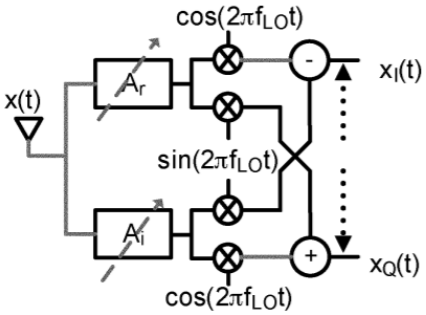

Figure 6: 90° phase shift in the form of complex down conversion [2].

The overall diagram of the two-antenna receiver can be shown in Figure 7 [2].

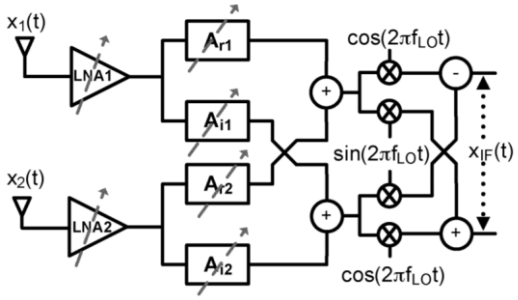

Figure 7: Proposed phased array receiver [2].

2.2.1 Receiver main blocks

The LNA is implemented using the common source inductive degeneration. The variable gain function is achieved by having a differential pair instead of cascade.

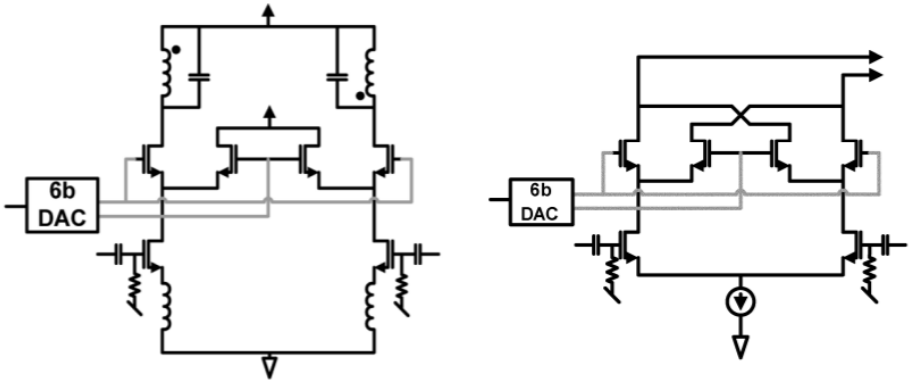

Figure 8: LNA implementation on left and VGA on the right [2].

The implementation idea of both VGA and the LNA [2] is taken from the idea of the multiplier as the input signal is fed to a differential pair and a 6b DAC is introduced to give the weighting function (multiplying the input signal with the output of the 6b DAC). Noting that since the gain of the VGA is needed to be invertible in sign the variable gain feature is implemented using a cross-coupled quad. Another important thing to be noted is that for each 2-antenna phased array receiver we have four mixers and two local oscillator signals that have 90° phase shift.

The weighted current output from the "real part" amplifiers are summed in the current domain and is fed into a primary winding of a three-winding transformer. The secondary winding is connected to 2 gilbert cells that are controlled by quadrature phases of local oscillators. The same is applied to the output weighted current from the "imaginary part" amplifiers. This can be shown in Figure 9.

The drawback of this receiver is that it is able to detect only one baseband stream at a time (support reception of 1 co-channel data stream at a time).

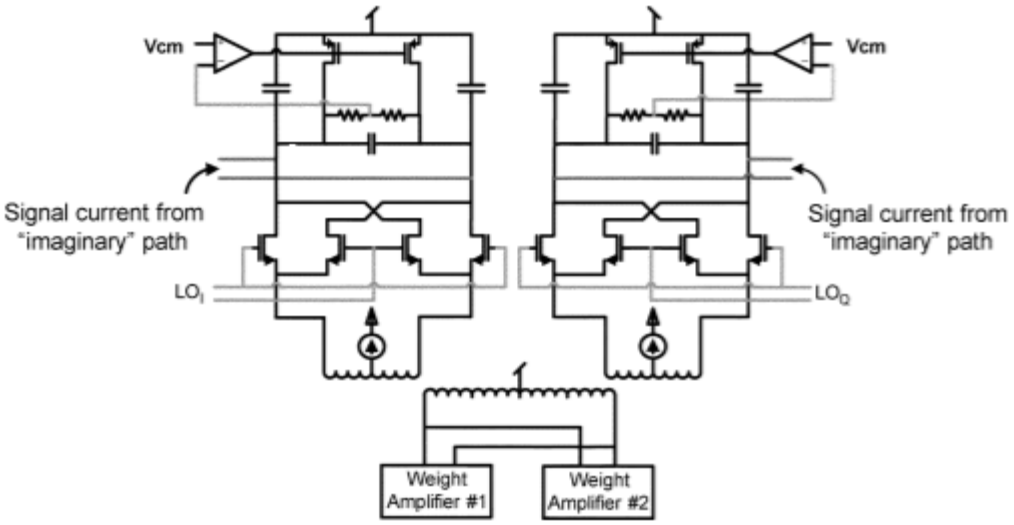

Figure 9: Current summation and gilbert cell stage [2].

This prototype was implemented using a 90-nm CMOS process.

2.3 Eight antenna 2-stream hybrid beamforming receiver

The architecture of this receiver is based on the cartesian combining receiver that was discussed earlier with the difference that it supports multiple baseband streams and it is a heterodyne down conversion receiver [3].

The receiver that is proposed by [3] is extended to support 8 antennas and is able to detect two-bit streams. The N-element/2-stream cartesian combining architecture require 4N PGA's and 2 complete down converting chain. This can be shown in Figure 10.

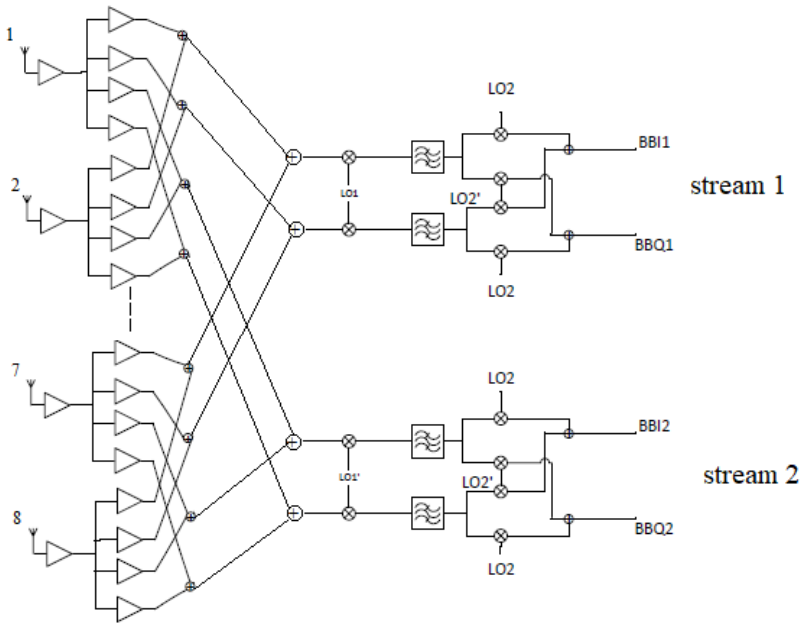

Figure 10: 8-antennas 2-stream beamforming receiver

2.3.1 Receiver main blocks

The LNA used in this receiver is the gain boosted common gate stage [3]. The common gate LNA is better than the common source because of the fact that the resistive input impedance is realized as 1/gm of the input transistor. Also, the fact that the induced gate noise of the input of the common source transistor may be significant. So, compared to common source LNA, the common gate LNA features broadband input matching, linearity and stability. To reduce the NF of the common gate LNA, an inverting gain is connected between the gate and the source. This is done here by the form of a transformer with turn ratio equal to n and coupling coefficient K.

$$n = \sqrt{{Ls}/{Lp}} \quad \& \quad K = \frac{M}{\sqrt{LS\ LP}} \tag{14}$$

Here LS and LP are the secondary and primary inductances, and M is mutual inductance.

Another two transformers are used at the output of the LNA, one to improve gain of the LNA and another one to provide single ended to differential output.

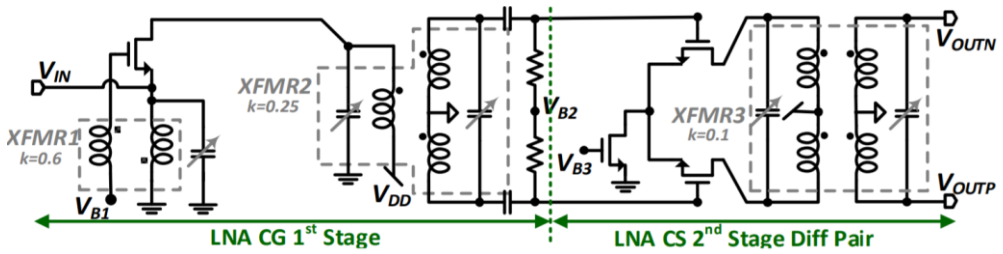

Figure 11: LNA implementation [3].

In the PGA implementation [3], 4-bit binary-weighted array of differential pair cells is used to realize an effective programable transconductance. Those cells are digitally controlled. The aim is to cover full 360° phase rotation. The unit GM cell consists of:

- Two identical differential pairs block (A and B) are connected with opposite polarity to invert the sign of the gain.
- One negative resistance block (block D) to keep load impedance constant for varying gain (when a cell is turned on, its finite output conductance changes the overall load impedance)
- To keep input capacitance of the PGA constant which ensures constant load capacitance for the LNA, a dummy differential pair (block C) is turned on when the whole cell is turned off.

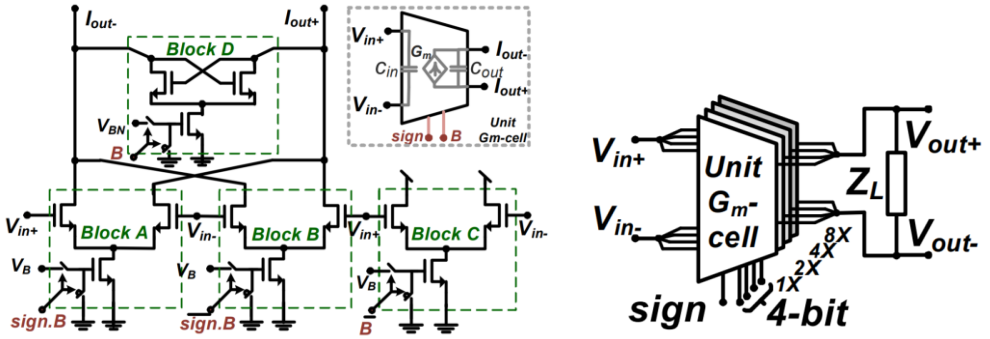

Figure 12: Digital controlled 4 bit cells and the schematic for a unit cell [3].

The weighted signal from the eight antennas are combined prior to quadrature downconversion using two combining stages as shown in Figure 10. In the first stage, outputs from corresponding PGA GM cells (that follows the LNA in Figure 10) are summed in the current domain this is done by connecting two GM-cells to a common transformer coupled load. This perform gain scaling and combining at the same time.

The second combining stage also uses current mode combining to a transformer couple load. After this combining stage, we will have Real and imaginary part for each stream.

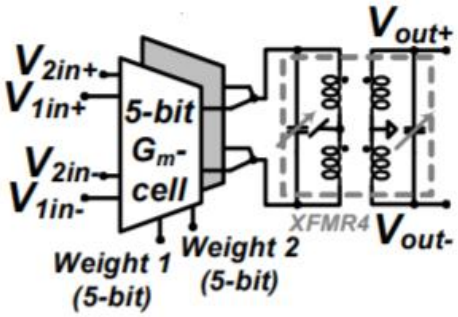

Figure 13: first combining stage [3].

Mixing in the two stages of the heterodyne receiver is done by pseudo differential double balanced gilbert cell mixer. The combining operation in the second mixing stage is realized by summing currents from buffer GM-cells to a resistive load.

This prototype was implemented using a 65-nm CMOS process.

2.4 Beamforming receiver with constant-GM vector modulators

Another cartesian vector modulator-based receiver is introduced in this section. The vector modulator is a combined phase shifter/amplitude modulator that in general depends on adding multiple copies of the input signal with different phase shifts and amplitude gain.

In a cartesian vector modulator, a set of four basis signals having phases of 0,90,180 and 270 are first generated. To have those phases we can use the in phase and quadrature outputs of a passive mixer as well as the negative counterparts in a balanced structure. Then a variable transconductors are used to scale the signals from the mixer output and sum into a point.

In order to minimize the problem of having gain and phase errors from the variable transconductors, constant GM vector modulator is used which uses a fixed bank of N binary scaled transconductances [4]. A set of configurable switches are used at the input of the transconductors, those switches allow the choice between the four signals at the output of the mixer. I+, I-, Q+. Q-.

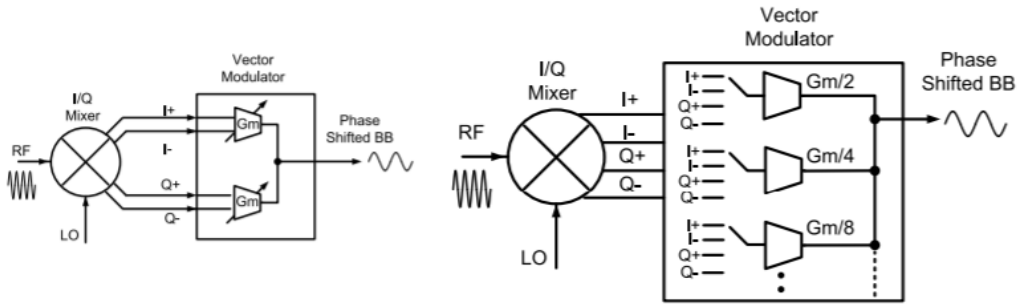

Figure 14: Constant GM vector modulator [4].

The advantage of the constant GM vector modulator is that for any constellation point, the same number of transconductances is enabled. This translates into equal loading of all circuit nodes.

The constant GM vector modulator as shown in Figure 14 has the drawback that we have large bank of transconductors (4 duplicated sets of transconductors are required for the four mixer phases). The idea of the receiver is to share the transconductors between the mixer phases and moved to the RF side. The operation as constant GM vector modulator is enabled by subdividing both the mixer and the transconductor into multiple slices [4]. This is shown in Figure 15. The vector modulator transconductance at RF acts as a low noise amplifier (LNA) and provides the input matching at the RF input port.

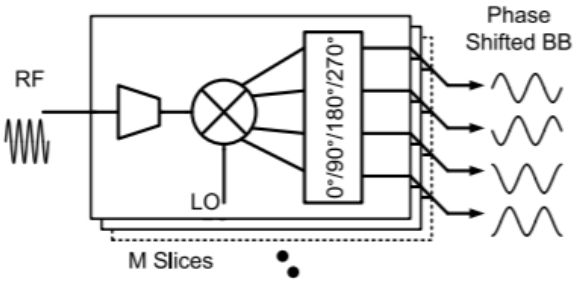

Figure 15: Proposed receiver architecture [4].

So, the implementation of this receiver requires transconductor, I/Q passive mixer with non-overlapping clock phases (25% duty cycle) and reconfiguration switches.

The implementation of the LNA is done based on an inverter with a resistive feedback to improve the noise figure and it will be discussed in more details in Chapter 4. Then the output of the LNA is AC coupled to the passive mixer. This passive mixer is consisting of four NMOS transistors. Each transistor has at gate a non overlapping signal with duty cycle of 25%. The output from those mixers are the I+, I-, Q+. Q- signals. The passive mixer will be discussed in more details in Chapter 5.

The slices shown in the Figure 15 are expanded into the full beamforming receiver by copying them into different branches and connecting them to baseband capacitance node. The currents from the antenna elements are summed into a summing node and filtered by this common baseband capacitance. The receiver architecture can be shown Figure 16 [4].

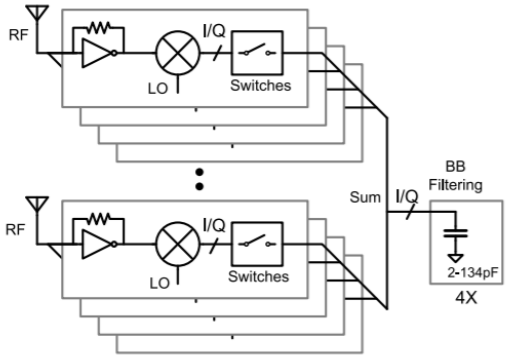

Figure 16: Receiver architecture [4].

For a 16x16 phasor constellation, 15 slices are needed for every antenna element with each slice providing $1/15^{th}$ of the input matching.

The baseband currents are sometimes out of phase for the unwanted received signal (spatial filtering in beamforming), so they are partially cancelled, and the baseband voltage swing is reduced. Since the passive mixer also has a bidirectional behaviour, the baseband voltage will be upconverted to the output node of the LNA. This up converted voltage has also low voltage swing in this case leading to increase in the IIP3.

2.5 Wideband scalable beamforming receiver

The receiver architecture introduced in this part is the one this thesis is taking a closer look at. The main idea of this receiver [5] is to introduce the scalable solution in the cases when we have large number of antennas for example 64. It is shown in Figure 17.

The IF module has two inputs from the two PGA, the output from these two amplifiers will be first down converted to the IF band of frequency of 2-4 GHz . The complex weighting that is needed in the beamforming receiver is achieved by having this PGA which introduce a variable amplitude in the RF side, while the 90 degree phase shift (needed in the complex weighting) is achieved by the cartesian combining (I/Q down conversion) in the IF module. The IF module slices are used for interference cancellation between multiple data streams.

The LNA and the passive mixer of this IF modules are under studies in this thesis. The aim is to see if we can take advantage of the parallelism to improve the linearity. The linearity is studied by building a polynomial model of the I-V curve of each block.

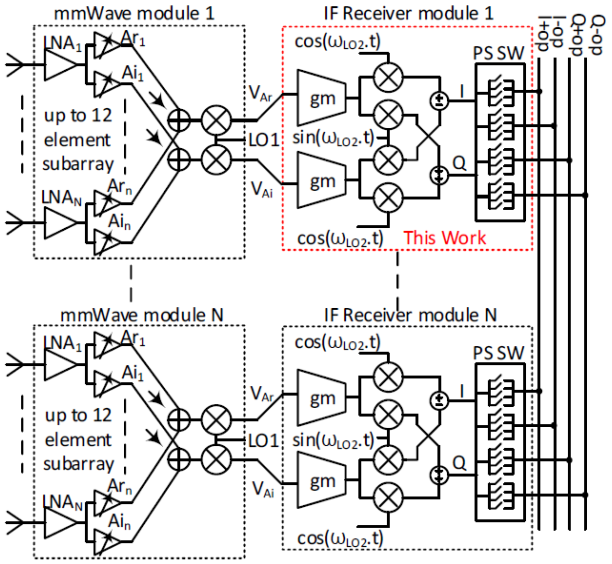

Figure 17: Receiver architecture [5].

The IF module of the receiver architecture is shown in Figure 17. The GM block is based on the inverter structure as introduced in the vector modulator receiver (introduced in section 2.4). The only difference here is that it is a pseudo differential pair structure. The GM block in this IF module is DC coupled to the quadrature passive mixer, unlike the vector modulator receiver introduced earlier where the GM block is AC coupled to the passive mixer. Instead a common mode feedback circuit is connected to the output of the GM block to set the common mode output voltage. Then a quadrature passive mixer is used with 4 inputs from the local oscillator signal that are shifted by 90 degree to form the in phase and quadrature components. Then phase switches are used to add current contributions of slices at the virtual ground node of the

transimpedance amplifier (TIA). Then the output current passes through a TIA which provides both the I-V conversion and the baseband low pass filtering [5].

It is important to note that, the previously stated receiver idea is based on the sawless filter receivers. The old conventional narrow band receiver makes a use of the off-chip saw filter. The saw filter in such receivers is placed after the antenna to block the large out of band signals (blockers) before it reaches the LNA. After that the LNA provide enough voltage gain at the wanted frequency, this helps to improve noise figure of the whole receiver. The presence of the saw filter relaxes the requirements for the linearity of the receiver (gain compression and intermodulation), reciprocal mixing (due to phase noise of the LO), harmonic mixing (due to square wave LO signal) and noise folding. At the same time this filter is an external filter which is bulky which require an extensive routing that could even corrupt the sensitivity or demand a lower NF to compensate the losses associated to long lines. This filter also is not tuneable which in some cases make us need large numbers of it. The cost is therefore high.

So, the aim is to remove the saw filter and at the same time not get harmed by the consequences of the receiver linearity and reciprocal mixing problems. The receiver doing this is called blocker tolerant receivers. Those receivers must avoid voltage gain at blocker frequencies and should generate LO signals with very low phase noise. A number of innovative designs have shown that a wide band CMOS front-end can tolerate blockers as large as 0 dBm[12]-[19]. Most of those receivers have two common features: they employ passive mixers and they suppress voltage gain at the blocker frequency. For example, passive first mixer implementation in [12]. This approach results in an exceptionally linear receiver while the noise figure is a bit high. Another receiver design utilizes a voltage sampling mixer to attenuate out of band signals by employing N-path filtering. **The other solution** is to replace the normal LNA with a transconductance LNA that drives a current mode passive mixer followed by a TIA. In such case, most of the voltage gain is moved to BB after a certain amount of filtering has occurred.

3 MODELING OF NONLINEAR BLOCKS

In this part, nonlinear systems are introduced and some proposed ways of measuring the nonlinearity. In general, passive components like resistors are linear while the active components like transistor is not. The linearity of the RF transmitter is very important for the transmitted signal with amplitude modulation for example (QAM). The nonlinear behaviour in the transmitter leads to the degradation in signal quality and makes it difficult for the receiver to recover the signal. Linearity of the receiver also is essential because the received signal has normally low power and if we have two blockers with high power entering a nonlinear LNA, the third order intermodulation product of the these two blocker may fold in the desired signal frequency and if the third order intermodulation product of the LNA is not low enough compared to the signal level (difference of 30 dB), the received signal will not be recovered properly.

3.1 Nonlinear systems

System is said to be linear if the output has a straight-line relationship with the input [6]. The straight line has a slope which is called gain and is not affected by the level of the input signal. While the nonlinear systems are the systems at which the input and the output have a curved relationship and the gain is affected by the level of the input signal. This can be show in Figure 18.

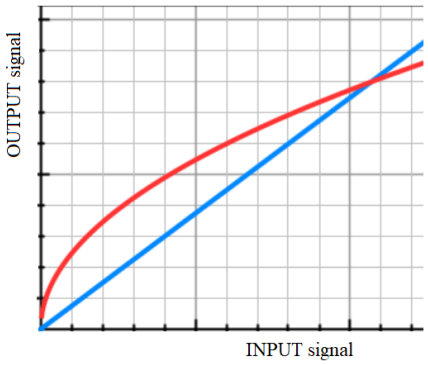

Figure 18: Linear and nonlinear systems.

3.2 Single and double frequency excitation of the nonlinear system

Firstly, we will discuss a single tone excitation to the nonlinear system [7] and see the spectrum of the output signal. We will assume that we have a sinusoidal source at a frequency w1 and has an amplitude A. When the input signal amplitude increases, the output signal spectrum will not only contain the fundamental frequency, but it will have also some higher harmonics. Now let's assume that the relationship between the input and the output is given by Taylor series (which is going to be explained latter in detail) as shown in the following equation.

$$y(t) \approx K_0 + K_1 x(t) + K_2 x(t)^2 + K_3 x(t)^3 + K_4 x(t)^4 + K_5 x(t)^5 + \cdots \quad (15)$$

where, K_1 is the first order coefficient, K_2 is the second order coefficient and K_3 is the third order coefficient and so on.

If $x(t) = A_1 \cos(w_1 t + \alpha_1)$ (single tone excitation, then the output can be shown in the following equation.

$$\begin{aligned} \mathrm{y(t)} \approx\ & K_0 + K_1 A_1 \cos(w_1 t + \alpha_1) + K_2 {A_1}^2 \left(\frac{1}{2} + \frac{1}{2}\cos(2w_1 t + 2\alpha_1)\right) \\ & + K_3 {A_1}^3 \left(\frac{3}{4}\cos(w_1 t + \alpha_1) + \frac{1}{4}\cos(3w_1 t + 3\alpha_1)\right) \\ & + K_4 {A_1}^4 \left(\frac{3}{8} + \frac{1}{2}\cos(2w_1 t + 2\alpha_1) + \frac{1}{8}\cos(4w_1 t + 4\alpha_1)\right) \\ & + K_5 {A_1}^5 \left(\frac{5}{8}\cos(w_1 t + \alpha_1) + \frac{5}{16}\cos(3w_1 t + 3\alpha_1) + \frac{1}{16}\cos(5w_1 t + 5\alpha_1)\right) \end{aligned} \quad (16)$$

The spectrum will be shaped according to Figure 19 [7].

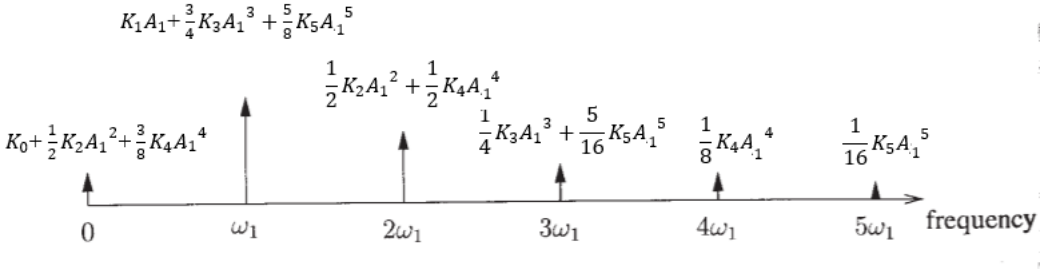

Figure 19: Output spectrum of nonlinear system due to single tone excitation.

It is observed that the third order nonlinear behaviour is giving additional component at the fundamental frequency. Because of that the fundamental response can increase faster than the linear response. This is called gain expansion. On the other hand, if the contribution from the third order term is to reduce the fundamental response in comparison to the linear response then this case is called gain compression. An important conclusion is that when the input signal changes the sign, the sign of the fundamental and the third harmonic changes, but not the second harmonic. This property is very beneficial in the balanced circuits as the differential output signal will not contain second order harmonics or other higher even order harmonics.

A good measure for the nonlinearity is harmonic distortion which can be calculated by the ratio between the nth harmonic response and the fundamental response. This can be applicable on our previous example (single tone excitation) as in the following equation [7].

$$HD2 = \frac{0.5\, K_2 {A_1}^2}{K_1 A_1} = \frac{1}{2} A_1 \left|\frac{K_2}{K_1}\right| \quad (17)$$

$$\mathrm{HD3} = \frac{0.25\, K_3 {A_1}^3}{K_1 A_1} = \frac{1}{4} {A_1}^2 \left|\frac{K_3}{K_1}\right| \quad (18)$$

Another measurement for the nonlinearity is the intercept points. Since the fundamental response is increasing linearly with the input while the second and the third harmonics at the output increases with the square and the cube of the input amplitude, the extension of both curves (fundamental and 2nd harmonic and the 3rd harmonic) are going to intersect at asymptotic points called 2nd order and 3rd order intercept points. Figure 20 shows when sweeping the input level from small to high values, how it will affect output fundamental and harmonic components [7].

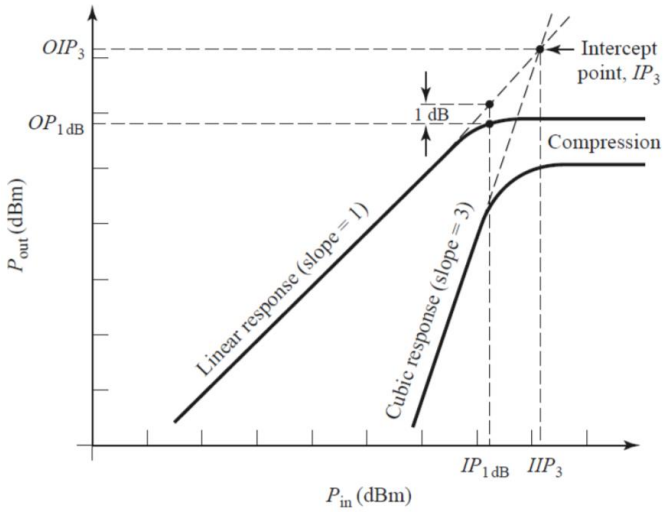

Figure 20: 2nd and 3rd order intercept point [7].

The higher the intercept point the better because this means that the 2nd and 3rd harmonics are small for moderate input amplitudes. The input level which is corresponding to the intersection of the harmonic and the fundamental is called the input intercept point.

Compression point is another way of measuring the nonlinearity. From Figure 20, it can be seen that when the input amplitude reaches a certain level, the gain degrades. This is called gain compression. 1-dB compression point is the input level at which the fundamental response is 1-dB less than its linear response, while 3-dB compression point is the input level at which the fundamental response is 3-dB less than its linear response.

Total harmonic distortion could also be used to measure the nonlinearity. If we have a sine wave input to a nonlinear system, the THD is a measure of how pure the output sine wave is. This can be done by measuring the amount of energy in the harmonics relative to the energy in the fundamental.

Secondly, in the case of the two-frequency excitation [7] we have two input signals $x(t) = A_1 \cos(w_1 t + \alpha_1) + A_2 \cos(w_2 t + \alpha_2)$. Due to the nonlinearity of the system, the two excitations will produce interfering signals in company with the harmonics of the two input signals. For example, the signals at the frequency $|w1 \mp w2|$ are formed due to the 2nd order nonlinear behaviour and are called second order intermodulation products. While signals at frequencies $|2w1 \mp w2|$ and $|w1 \mp 2w2|$ are formed due to the 3rd order nonlinear behaviour and are called third order intermodulation products. The only difference is that the signals at frequencies $|2w1 \mp w2|$ increases with the square of A_1 and with first power of A_2 while signals at frequencies $|w1 \mp 2w2|$ increases with first power of A_1 and with the square of A_2. The spectrum due to the excitation from two tones can be shown in Figure 21.

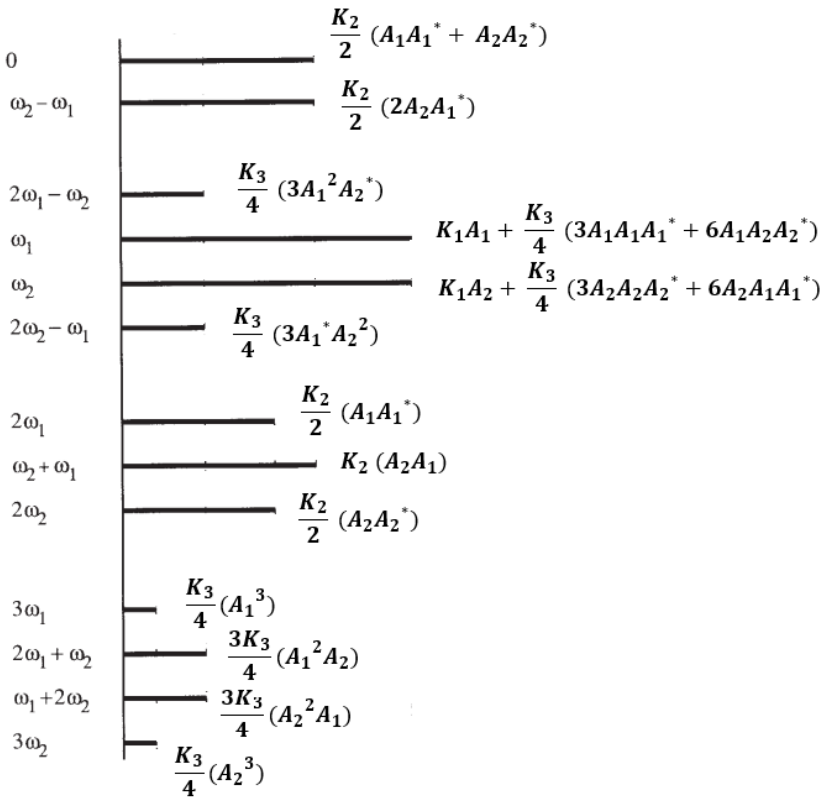

Figure 21: Harmonic and intermodulation products due to two tones excitation.

The nth order intermodulation distortion (IM_n) is the ratio between the nth order intermodulation response to the fundamental response. From our previous example (the two tones excitation), IM_2 and IM_3 can be calculated as in the following equations [7].

$$IM_2 = \frac{K_2\, A_1A_2}{K_1A_2} = \left|\frac{K_2}{K_1}\right| A_1 \tag{19}$$

Here, the fundamental response is taken at w_2 and the intermodulation response at frequency $(w_2 + w_1)$.

$$IM_2 = \left|\frac{K_2}{K_1}\right| A_2 \tag{20}$$

In this equation, the fundamental response is taken at w_1 and the intermodulation response at frequency $(w_2 - w_1)$. The two intermodulation distortions are equal in case of the input amplitude of the two tones are equal.

Similarly, the 3rd order intermodulation distortion can be calculated according to the following equation. The fundamental response is taken at w_1 and the intermodulation response at frequency $(2w_1 - w_2)$.

$$IM_3 = \frac{3}{4}\left|\frac{K_3}{K_1}\right| A_1\, A_2 \tag{21}$$

The third order intermodulation response could arise by mixing second order products at the second harmonic or the difference frequency with the fundamental response. For example, $\mathrm{V}(2w_1) * \mathrm{V}(w_2)$ or $\mathrm{V}(w_1) * \mathrm{V}(w_1 - w_2)$.

The intercept points in the case of two tones takes into account the 2nd and the 3rd order intermodulation products and not only the harmonics. The IIP3 in this case is the input level corresponding to an asymptotically point, which comes from the intersection of the extension of the curves of intermodulation products at the frequencies $(2w1 - w2)$ and the fundamental response.

3.3 Modelling of Nonlinear systems

The purpose of modelling the nonlinear systems is to know the dominant causes of nonlinearities in the circuit, hence we could determine the possible ways of reducing it. This valuable information cannot be obtained by the circuit simulators as they will provide the total amount of distortion.

3.3.1 Taylor series

The circuit non-linearities can be expand in Taylor series. This can be done over a certain bias point. For example, the drain to source current (i_{DS}) of the MOSFET transistor at a given fixed (v_{DS}) can be written as a function of the (v_{gS}) as in the following equation [7].

$$i_{DS}(v_{GS}) \approx i_{DS}(V_{GS}) + K_1 v_{gs} + K_2 {v_{gs}}^2 + K_3 {v_{gs}}^3 + \cdots \tag{22}$$

Here, the uppercase symbols as V_{GS} denotes to the bias voltages and the lowercase symbols as v_{gs} denote small signal deviation while v_{GS} is the total gate to source voltage which is the sum of the V_{GS} and v_{gs}. A multi-dimensional case will be discussed later in Section 3.3.3.

As can be seen in the previous equation that we can model the non-linearity of the device as a series of terms from the DC up to the third order term. The coefficients can be calculated according to the following equation.

$$K_n = \frac{1}{n!} \frac{d^n i_{DS}}{d {v_{gs}}^n} \tag{23}$$

Taylor series is fitting well when the input is small while in case of having large input, Taylor series has problems. There are two main problems associated with Taylor series which are the limited convergence domain and the error behaviour.

Taylor series has a convergence domain that is a disk in complex domain [8]. The disk has a radius called radius of convergence. This radius is from the expansion point (operating point) up to a singularity complex point and it can be determined by ratio test. This implies that for some values of v_{gs} the polynomial function will not converge.

The other problem of Taylor series is that it has a residual function (error function). This error function is very small around the expansion point and is huge when the distance from that point increases. This happens for example when we have a large input signal. In this case more terms are needed to reduce the error.

3.3.2 VOLTERRA SERIES

Volterra series describes the output as sum of operators that are applied on the input. This can be shown in Figure 24.

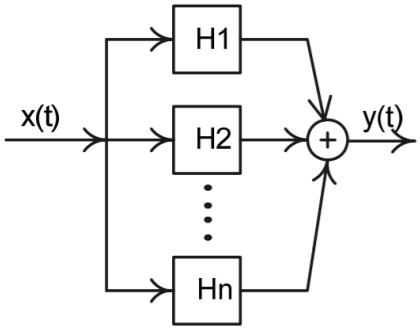

Figure 22: Diagram of Volterra series.

The operator performs a transformation of the input signal to produce an output signal. the operators can be first (linearized response), second and third order Volterra operator and has notation H_1, H_2 and H_3 respectively. As the input amplitude increases, higher order nonlinear effects occur so more higher order operators are needed [7].

Consider having a second order nonlinear system, its operation is to combine two signals that are identical. For example, if we have a single tone input with frequency w_1, the second order nonlinear system will produce the multiplication of two multiples of the input signal so that the output signal has two frequency components, one at ($w_1 + w_1 = 2w_1$) and the other at ($w_1 - w_1 = 0$). Another example, if we have two tones input signal with frequencies w_1 and w_2 that are input to a second order nonlinear system, the second order nonlinear system will produce the multiplication of the two input signals so that the output signal will have frequency components at frequencies ($w_1 + w_2$) and ($w_1 - w_2$). The nonlinearity will also produce the multiplication of two multiples of the signal at w_1 and the multiplication of two multiples of the signal at w_2 so the out signal will have frequency components at DC, $2w_1$ and $2w_2$. The same concept can be applied to the third order nonlinear system.

Volterra series has the advantage that it takes the memory effect into account that comes from the inductors and capacitor in high frequency, unlike Taylor series.

3.3.2.1 Volterra series expansion

In this part we will try to come up with an expression for the Volterra series. For the system with memory and has first order nonlinearity, we can describe the output by summing all the effects of the past input with proper weighting. This will give the linear discrete response as in the following [7].

$$y(n) = \sum_{i=0}^{n} h(\tau_i)x(n - \tau_i) \tag{24}$$

where, $h(\tau)$ is the impulse response.

For the continuous time domain system, the equation will be in the form of convolution integral.

$$y(t) = \int_0^t h(\tau)x(n-\tau)dt \tag{25}$$

For the system with second order nonlinearity that is discrete and with memory the output can be described as in the following equation.

$$\begin{aligned} y(n) &= x(n)x(n) + x(n)x(n-1) + \cdots + x(n)x(0) \\ &+x(n-1)x(n-1) + x(n-1)x(n-2) + \cdots + x(n-1)x(0) + \cdots + x(0)x(0) \end{aligned} \tag{26}$$

$$y(n) = \sum_{i=0}^{n}\sum_{J=0}^{n} x(i)x(j) \tag{27}$$

Adding a proper weighting to form a weighted double sum.

$$y(n) = \sum_{i=0}^{n}\sum_{J=0}^{n} h_2(p_i, p_j)x(n-p_i)x(n-p_j) \tag{28}$$

where, $h_2(p_i, p_j)$ is the second order impulse response with time index (p_i and p_j). It is known also as second order Volterra kernel.

For the continuous time domain, the equation will be

$$y(t) = \iint_0^t h_2(\tau_1, \tau_2)\, x(t-\tau_1)\, x(t-\tau_2)d\tau_1 d\tau_2 \tag{29}$$

As a conclusion the Volterra series expansion for a nonlinear system is the summation of infinite multidomain convolution integral.

$$\begin{aligned} y(t) &= \int_0^t h(\tau)x(t-\tau)dt + \iint_0^t h_2(\tau_1, \tau_2)\, x(t-\tau_1)\, x(t-\tau_2)d\tau_1 d\tau_2 + \cdots \\ &+ \int \dots \int_0^t h_n(\tau_1, \dots, \tau_n)x(t-\tau_1) \dots . x(t-\tau_n)d\tau_1 \dots . d\tau_n \\ &= H_1[x(t)] + H_2[x(t)] + H_3[x(t)] + H_4[x(t)] + \cdots + H_n[x(t)] \end{aligned} \tag{30}$$

The frequency domain representation can be done by taking the Fourier transform of the Volterra kernel.

$$H_{\mathrm{n}}(jw_1, jw_2, \dots, jw_{\mathrm{n}}) = F[h_n(\tau_1, \dots, \tau_n)] \tag{31}$$

Then the output of the nth order nonlinear system is

$$\mathrm{Y} = H_1(jw_{\mathrm{p1}})\, X + H_2(jw_{\mathrm{p1}}, jw_{\mathrm{p2}})\, X^2 + \cdots + H_{\mathrm{n}}(jw_{\mathrm{p1}}, \dots, jw_{\mathrm{pn}})\, X^n \tag{32}$$

where, w_{p1}, w_{p2},…., w_{pn} can be chosen from $\mp w_1$, $\mp w_2$,… $\mp w_{\mathrm{n}}$.

In the next part we will introduce a comparison between Taylor series and Volterra series in some points of comparison. Assume that we have a nonlinear system with two tone inputs with frequencies equal to w_1, w_2 and amplitude A.

Table 1: HD and IM comparison between Volterra and Taylor series.

Point of comparison	Volterra series	Taylor series
HD2	$\frac{1}{2}\left\lvert\frac{H_2(jw_1,jw_1)}{H_1(jw_1)}\right\rvert A$	$\frac{1}{2}\frac{a_2}{a_1}A$
HD3	$\frac{1}{4}\left\lvert\frac{H_3(jw_1,jw_1,jw_1)}{H_1(jw_1)}\right\rvert A^2$	$\frac{1}{4}\frac{a_3}{a_1}A^2$
IM2	$\left\lvert\frac{H_2(jw_1,jw_2)}{H_1(jw_1)}\right\rvert A$	$\frac{a_2}{a_1}A$
IM3	$\frac{3}{4}\left\lvert\frac{H_3(jw_1,jw_1,-jw_1)}{H_1(jw_1)}\right\rvert A^2$	$\frac{3}{4}\frac{a_3}{a_1}A^2$

One way of finding the Volterra kernel is by the harmonic substitution method. For example, if we have a differential equation of a series inductor, resistor and nonlinear resistor as show in the following equation.

$$L\,y'(t) + R\,y(t) + R_n y^2(t) = x(t) \tag{33}$$

To find $H_1(s_1)$, let $x(t) = \exp(s_1 t)$ and $y(t) = H_1(s_1)\exp(s_1 t)$ and then equate the coefficients of $\exp(s_1 t)$ on both sides. This will give us

$$H_1(s_1) = \frac{1}{s_1 L + R} \tag{34}$$

To find $H_2(s_1, s_2)$, let $x(t) = \exp(s_1 t) + \exp(s_2 t)$ and $y(t) = H_1(s_1)\exp(s_1 t) + H_1(s_2)\exp(s_2 t) + 2H_2(s_1, s_2)\exp(s_1 + s_2)t$ and then equate the coefficients of $2!\exp(s_1 + s_2)t$ on both sides. This will give us

$$H_2(s_1, s_2) = R_n H_1(s_1) H_1(s_2) H_1(s_1 + s_2) \tag{35}$$

3.3.3 Polynomial modelling

The main idea is to model the nonlinearity in the device with a polynomial function of their controlling ac voltages and junction temperature. For example, in the MOS transistor i_{DS} can be modelled as in the following equation as function of v_{gs} , v_{ds} and t_{j} [9].

$$\begin{aligned} i_{\mathrm{DS}} = {} & K_{100}\,v_{\mathrm{gs}} + K_{200}\,{v_{\mathrm{gs}}}^2 + K_{300}\,{v_{\mathrm{gs}}}^3 \\ & + K_{010}\,v_{\mathrm{ds}} + K_{020}\,{v_{\mathrm{ds}}}^2 + K_{030}\,{v_{\mathrm{ds}}}^3 \\ & + K_{110}\,v_{\mathrm{gs}}\,v_{\mathrm{ds}} + K_{210}\,{v_{\mathrm{gs}}}^2\,v_{\mathrm{ds}} + K_{120}\,v_{\mathrm{gs}}\,{v_{\mathrm{ds}}}^2 \\ & + K_{001}t_{\mathrm{j}} + K_{101}\,v_{\mathrm{GS}}\,t_{\mathrm{j}} + K_{011}\,v_{\mathrm{DS}}\,t_{\mathrm{j}} \end{aligned} \tag{36}$$

where, K_{nmp} are the coefficients of the polynomial and the index refers to the product terms ${v_{\mathrm{GS}}}^n\ {v_{\mathrm{DS}}}^m\ {t_{\mathrm{j}}}^p$.

Fitting the polynomial model (finding the coefficients) can be done in many ways. If we have the measured or the simulated data, we can easily extract the vector of the coefficients by dividing the model by the measured data.

The classical method is to get the higher order derivatives of the nonlinear function at the bias point, but this will have same problems as in the Taylor series. So, the input signal amplitude is needed to be small (when the signal amplitude increases, more coefficients needed to reduce the remainder function).

Another more practical method is to make the value of the coefficients changeable with the signal amplitude [10]. This can be done by expressing the higher order components using the residual term of the Taylor series.

$$R_n(x) = \frac{1}{n!}\int_0^x (x-t)^2 f(t)dt \tag{37}$$

Equation (37) works nicely for point values of x, but in distortion analysis x is a function of time. Hence, Rn needs to be evaluated at all time points of one cycle of a sine wave.

Fitting of the polynomial model can also be done as in [22]. The technique is based on simulated large signal voltage and current spectra. This approach would be very helpful when the polynomial expansion needs to be calculated from experimental or simulated data.

The nonlinearity coefficients can also be calculated using a different type of polynomial expansion, the Chebyshev series as shown in [8].

3.3.3.1 Comparison between Taylor and polynomial

Finally, Figure 23 shows the drain current of 45nm technology MOSFET (VT = 0.5, W = 200µm, VDS = 1.5V) and it is associated 3-terms Taylor series with VT expansion point. The polynomial model fitting is done based on [23]. At which simulated data are used to extract polynomial coefficients values.

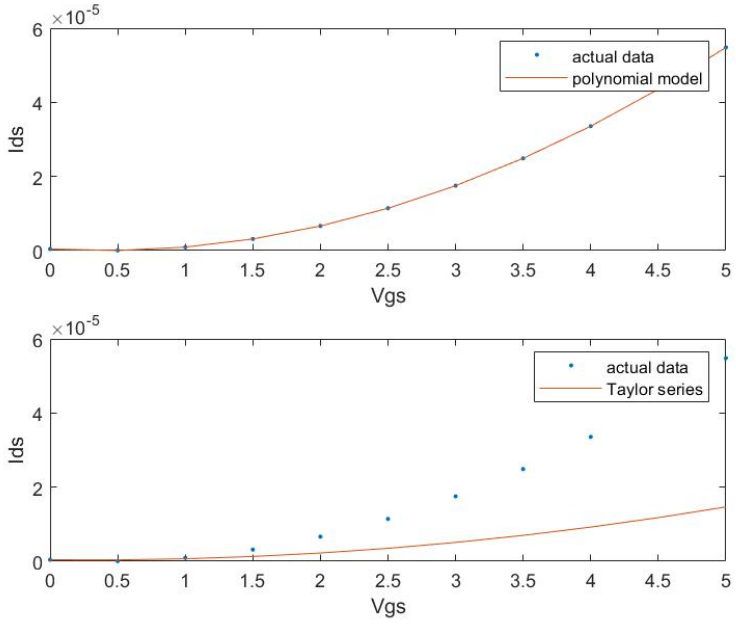

Figure 23: Taylor and Polynomial fitting comparison.

It is clear that Taylor series diverges as we go far from the expansion point. As the number of terms used for fitting increases the divergences happens far from the expansion point. While the polynomial fitting shows more convergence even for the high input voltages and that's why we are going to continue our analysis in the following chapters using the polynomial model.

4 ANALYSIS OF THE GM BLOCK

4.1 Receiver architecture

From the proposed receiver in Figure 17, we are going to analyse a single path in one slice of that receiver which has several similar slices in parallel. A single slice is shown in Figure 24.

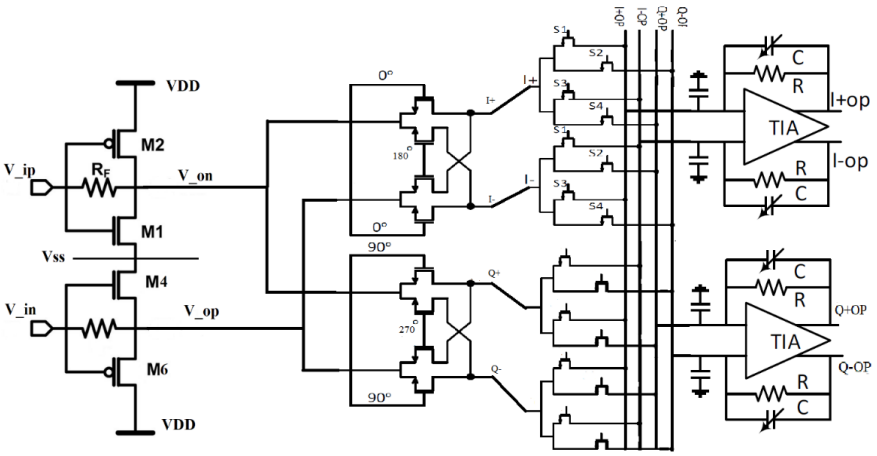

Figure 24: Single path of one slice of the proposed receiver

It is known that the RF receiver often needs to sense a weak desired signal along with a strong interferer. During the signals travelling in the receiver chain both the blocker and the signal are amplified. So, it is recommended to design the receiver circuit blocks with high linearity till the stage which filters the blocker. In general, as the voltage swing at each interface is minimized, the linearity improves. As a result, we contemplate the use of the current mode signals and low impedance levels to reduce the voltage swings.

The IF-Rx architecture has many parallel slices of this IF module. The summation of parallel branches is noncoherent for different noise sources, and coherent for signal sources. This is boosting up the noise performance. Distortion, however, is synchronous to the signal itself. It is known that differentiality cancels even order nonlinearity [20], but odd order nonlinearities sum up coherently just like the signal. That applies if the parallel branches are exactly similar. If they do have some minor differences, it may be that their nonlinearity varies, too, and the purpose is to see if that can be utilized for linearity improvement.

4.2 GM stage LNA block

Figure 24 shows a typical modern RF receiver, where both the signal and the blocker are sensed by the antenna that derives GM stage (voltage to current conversion) and then the output current is applied to a passive mixer to finally generate the baseband current. The Transimpedance amplifier set low impedance level at both the input and the output port of the passive mixer which result in improved linearity for both the GM stage and mixer stage. This means that we can tolerate the blocker until the input port of the TIA.

In this part, we are going to analyse the linearity of its block, starting with the GM block. CMOS inverter shown in Figure 26 has many applications in the digital and analog domain. In the analog domain, it can be used as VGA, LNA, transimpedance amplifiers and many other applications. For example, CMOS inverter as voltage amplifier gives gain if both transistors are

in saturation. For this to happen the operating point is at the point where input and output voltages are equal.

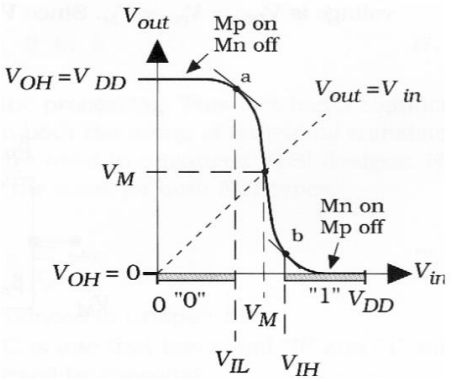

Figure 25: Input-Output voltage characteristics of CMOS inverter [20].

The open-loop, unloaded voltage gain can be calculated as the derivative (slope) at this point. The analysis is done with small signal because we need the signal to fit within this linear region. The voltage gain can also be calculated by superposition.

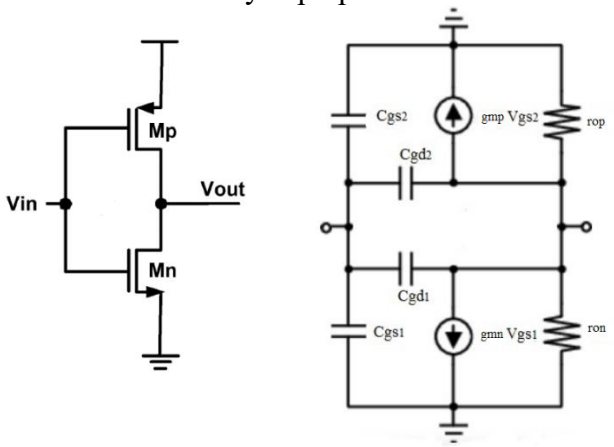

Figure 26: CMOS inverter and equivalent small signal model.

From superposition, we can find that the voltage gain is $-(gm_{\mathrm{n}} + gm_{\mathrm{p}})(r_{\mathrm{on}} \| r_{\mathrm{op}})$ at which $gm_{\mathrm{n}}, gm_{\mathrm{p}}$ are the transconductance of the NMOS and PMOS respectively while $r_{\mathrm{on}}, r_{\mathrm{op}}$ are the output resistance of the NMOS and PMOS transistor respectively. This indicates that both the NMOS and PMOS will contribute to the total gain.

The CMOS inverter in our receiver is used as a transconductance amplifier which acts as LNA and provides the input matching. The purpose of this transconductance amplifier is to transfer the input voltage into output current. This is a desired function as the addition from different slices in the receiver is easier in the current domain. Another important function of the transconductance amplifier is that it is used for the amplitude scaling of the input signal. The total transconductance of the GM block is $gm_{\mathrm{n}} + gm_{\mathrm{p}}$ = 5mS. The proposed LNA (GM block) is based on the shunt feedback amplifier.

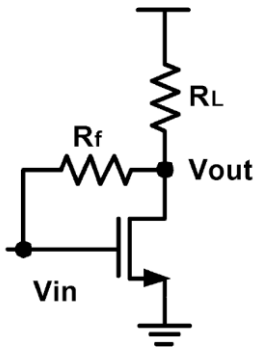

Figure 27: Shunt feedback amplifier principle.

The advantage of the shunt feedback topology is that a 6 dB NF could be achieved by $gm \geq$ 5mS while for the shunt input resistance amplifier to achieve noise figure of 6dB, gm needs to be larger than 25mS.

One technique that can be adopted to lower the power consumption is to reuse the current by stacking the NMOS and PMOS as amplifying devices. This can be shown in Figure 28 a PMOS on the top of NMOS which gives an overall GM $\approx gm_{\mathrm{n}} + gm_{\mathrm{p}}$ instead of only gm_{n}.

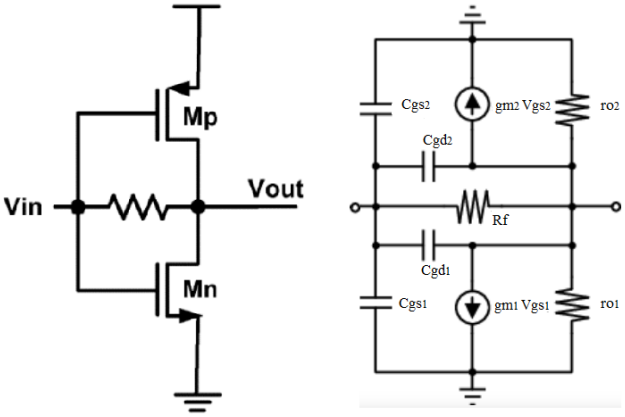

Figure 28:Current reuse technique for shunt feedback amplifier and its small signal model.

In the design of the low noise transconductance amplifier based on inverter, we should take care of many parameters. Those parameters should be optimized to get the desired requirements of low noise figure in range of 2dB, voltage gain is very low and high linearity (IIP3 of 4-7dBm) and it should provide the input matching.

Since the PMOS transistor has a lower carrier mobility than the NMOS transistor the width Wp of the PMOS should be larger than Wn. However, this depends on the technology used as in some technologies the carrier mobility of NMOS and PMOS are pretty close.

Increasing the gm value, decreases the rout of the transistor. The previous relation is important when we optimize the amplifier for the design requirements.

The bias of both transistors is set to be the same, where VG= VDD/2. The negative feedback resistor ensures a stable DC operating point and increases the bandwidth.

4.2.1 Noise analysis of GM stage

The thermal noise for the transistor is given by the following equation

$$v_n{}^2 = 4K_B T\gamma \frac{1}{gm} \tag{38}$$

where, K_B is boltzman constant, T is absolute temperature and γ is noise coefficient. From this equation, it is clear that an increase in gm value will reduce the thermal noise of the transistor. However, increasing gm means higher power consumption and wider width which limits the bandwidth.

An expression for the noise figure for schematic in Figure 27 can be concluded by calculating the noise from each device at the output and then add the RMS voltages as shown in the following steps.

Firstly, for the m1 transistor.

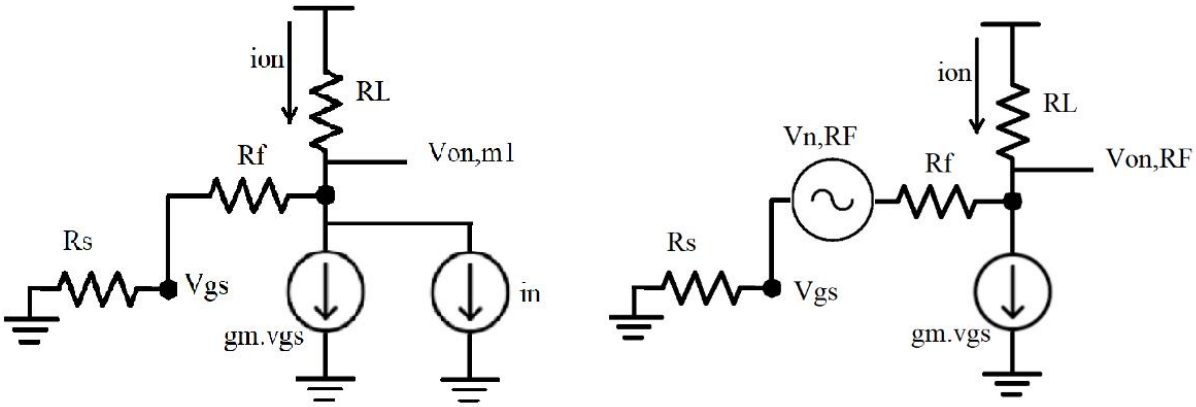

Figure 29: Schematics for calculating noise from m1 and Rf.

The output noise from the m1 can be calculated from Figure 29 on the left.

$$v_{on,m1} = \frac{i_n}{\frac{1}{R_L} + \frac{g_m R_s}{R_f + R_s}} \tag{39}$$

If $R_f \gg$ and $R_s \ll$ then the previous equation can be approximated to

$$v_{on,m1} \approx \frac{i_n R_f}{\frac{R_f}{R_L} + g_m R_s} \tag{40}$$

Secondly, for the Rf resistance, the output noise from the m1 can be calculated from Figure 29 on the right.

$$v_{on,Rf} = v_{n,Rf} \frac{g_m R_s + 1}{g_m R_s + 1 + \frac{R_s + R_f}{R_L}} \approx \frac{2R_L}{2R_L + R_f} v_{n,Rf} \tag{41}$$

Thirdly, for the Rs resistance.

$$v_{on,Rs} = v_{n,Rs}\ \frac{1}{2}\ A_V \tag{42}$$

where, $A_V = -g_m(R_f \| R_L)$. As $R_f \gg R_L$ and $g_m = \frac{1}{R_s}$ then $A_V \approx \frac{-R_f}{R_s}$

In practice g_m is not necessarily equals to $\frac{1}{R_s}$. This is just an assumption to make analysis easier. The g_m value in the receiver design is in range of 5 to 10 mS.

Then the total RMS output voltage is as shown in the next equation.

$$v_{out}{}^2 = v_{on,Rs}{}^2 + v_{on,Rf}{}^2 + v_{on,m1}{}^2 \tag{43}$$

The input referred noise can be calculated as in the following equation.

$$v_{ni}{}^2 = \frac{v_{out}{}^2}{\left(\frac{1}{2}A_V\right)^2} \tag{44}$$

$$v_{ni}{}^2 = 4KTR_s + \frac{4KTR_f R_L{}^2}{(R_L + \frac{R_f}{2})^2(\frac{-R_f}{R_s})^2/4} + \frac{4KT\gamma g_m R_f{}^2}{(\frac{R_f}{R_L}+1)^2.(\frac{-R_f}{R_s})^2/4} \tag{45}$$

$$NF = \frac{v_{ni}{}^2}{4KTR_s} = 1 + \frac{4R_f R_L{}^2}{R_s(R_L + \frac{R_f}{2})^2(\frac{-R_f}{R_s})^2} + \frac{4\gamma g_m R_f{}^2}{R_s(\frac{R_f}{R_L}+1)^2.(\frac{-R_f}{R_s})^2} \tag{46}$$

While for the cascaded structure in Figure 28, the noise figure can be calculated as in the following equation.

$$NF = \frac{v_{ni}{}^2}{4KTR_s} = 1 + \frac{4R_f R_L{}^2}{R_s(R_L + \frac{R_f}{2})^2(\frac{-R_f}{R_s})^2} + \frac{2(\gamma_1+\gamma_2) g_m R_f{}^2}{R_s(\frac{R_f}{R_L}+1)^2.(\frac{-R_f}{R_s})^2} \tag{47}$$

where $\gamma_1 and\ \gamma_2$ are the noise factor of NMOS and PMOS transistors respectively.

Equation 47 shows that the noise figure from a cascaded structure is less than the single structure. The cascaded structure also has more gain as the total Gm is $gm_{\mathrm{n}} + gm_{\mathrm{p}}$.

4.2.2 Matching of the GM stage

For input matching, the input resistance of the amplifier from the small signal model is calculated as in the following equation.

$$R_{\mathrm{in}} = \frac{1 + \frac{R_{\mathrm{f}}}{r_{\mathrm{on}} \| r_{\mathrm{op}}}}{gm_{\mathrm{n}} + gm_{\mathrm{p}}} \quad \& \quad S_{11} = \frac{R_{in} - R_s}{R_{in} + R_s} \tag{48}$$

It is important to note that the receiver proposed by [5] has 15 slices. So, each slice providing $1/15^{\mathrm{th}}$ of the input matching.

For the output matching, the output resistance also can be calculated from the small signal model as in the following equation.

$$R_{\text{out}} = r_{\text{on}} \| r_{\text{op}} \| \frac{R_{\text{f}} + R_{\text{s}}}{1 + (gm_{\text{n}} + gm_{\text{p}})R_{\text{s}}} \tag{49}$$

The voltage gain is given by the following equation.

$$A_{\text{v}} = -(gm_{\text{n}} + gm_{\text{p}})(r_{\text{on}} \| r_{\text{op}} \| Rf \| RL) \tag{50}$$

So, by optimizing the values of gm_{n},gm_{p}, Rf, r_{on}, r_{op} we can get any design requirements. Here we are interested in high linear Gm stage, so the Voltage gain is small. The feedback resistance is needed to be high to provide proper input matching. The GM value needs to have low power consumption.

4.2.3 GM stage properties and components value

The prototype we are looking is implemented using 28nm CMOS where the gate length (L) is 30nm, $Fmax$ is 250 GHz and the threshold voltage is approximately 0.35V. The Vdd value used in the design is 0.9V, Feedback resistance (Rf) is 3.5kΩ and the transistor sizing is done so that the Gm value is 5mS. The voltage gain provided by this circuit is very low as the output impedance is small.

In the proposed receiver [5], the input signal is differential so a pseudo differential transconductor pair structure is used by placing two gm paths in parallel. Here, there is often a need for cancelling the common mode signal which is done by measuring the average in the output and rejecting it with a feedback. This sets the common mode output of the pseudo differential gm block. It is also helpful to avoid operating point mismatch between the stages.

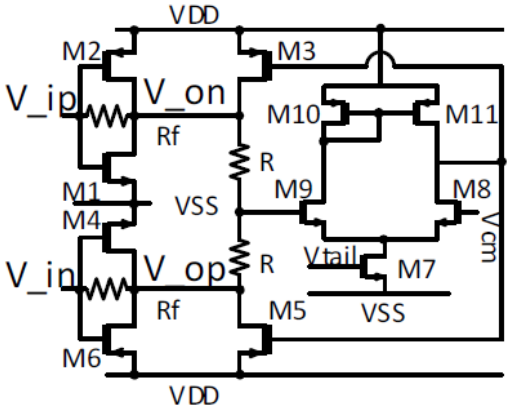

Figure 30: Pseudo differential transconductor pair with the common mode feedback stage [5].

The average output voltage is calculated at the input of M9, if it is high, it will produce current in the drain of M9. This current is going to be reflected to the other side by means of the current mirror formed by M10 and M11. This current will see a high impedance at the output of the differential pair which cause a high voltage that will drive M3 and M5 which are PMOS transistors so the current through both transistors will reduce and hence this will bring the common mode voltage down towards the reference Vcm given at the gate of M8 .

4.2.4 GM stage linearity analysis

In this part, we are going to study the linearity of the GM block. In order to do so we have the schematic shown in Figure 31.

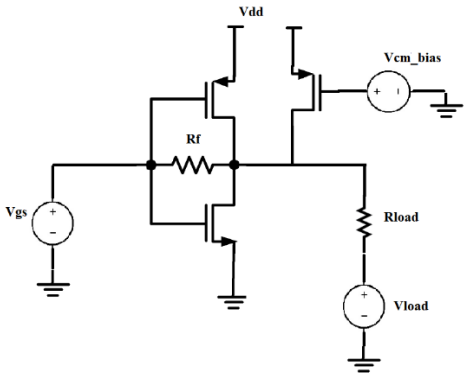

Figure 31: Circuit diagram used in schematic.

The output stage is loaded with the PMOS transistor used in the common mode feedback strategy in parallel with the load resistance (Rload). The desired operating point is happening when Vin = Vout = 0.45v, and the common-mode feedback has a fixed bias to achieve that. At this point both transistors are in saturation. Figure 32 shows the input voltage sweep against the drain voltage for different output voltages (load voltage).

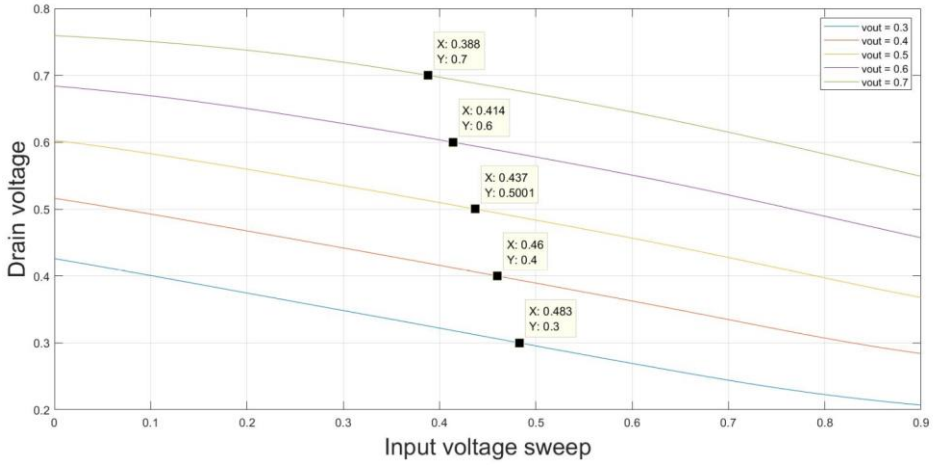

Figure 32: Drain voltage VS input voltage.

The marked points in Figure 32 represents the operating points at different output voltages.

The linearity of the GM block is studied by building the polynomial model of the I-V curve and studying the first, second and third order coefficients. This is done for two different cases, the first one when we have output resistance of 50 Ω and varying the output voltage (we vary the input voltage from 0V to 0.9V, steps up the output voltage from 0.3V to 0.7V and fix the load resistance to 50 Ω). The resulting curves are shown in Figure 33. The second one when we have output voltage (load voltage) that is 0.45V and we vary the output resistance (we vary the input voltage from 0V to 0.9V and steps up the output resistance from 50Ω to 1000Ω). The resulting curves are shown in Figure 34.

The aim is to know if there is a possibility of introducing minor offset in the output operating point of the parallel blocks shown in Figure 17 so that the 3rd order coefficient would have opposite sign. This would then cause some cancellation of distortion in the combined output.

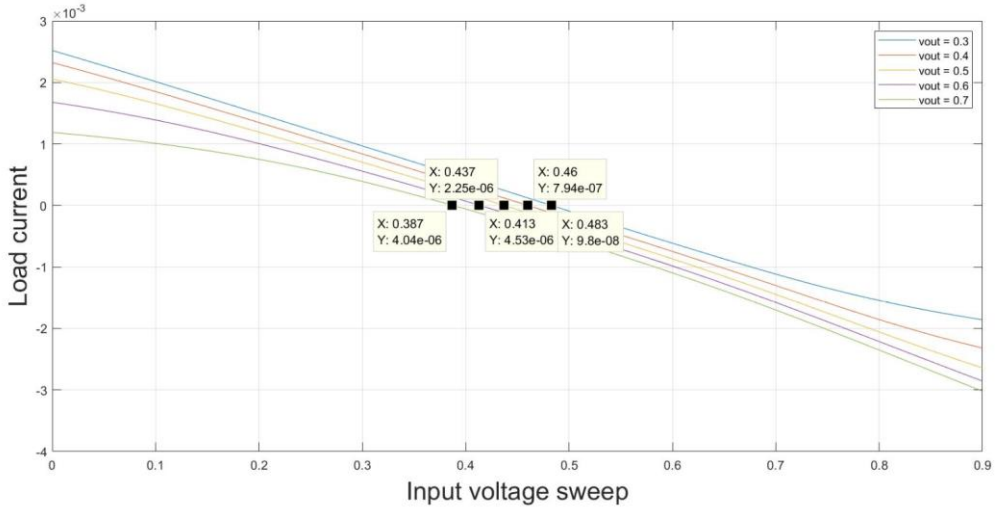

Figure 33: I-V curve of GM block at different output voltages.

The marked points also in Figure 33 represents the operating point

It is worth mentioning that the GM stage is DC-coupled with the passive mixer switches which means that the GM block is driving the mixer. The passive mixers have no reverse isolation as they are intrinsically bidirectional. This results in the interaction between the inputs and the outputs of the passive mixer. The voltage at the input RF port of the passive mixer is dependent on the baseband impedance at the output port and on the switching behaviour of the LO signal. The input resistance of the passive mixer also is dependent on the baseband impedance. The proposed receiver has a current mode passive mixer which is followed by a transimpedance amplifier. This transimpedance amplifier has low input resistance (few tens of ohms).

The aim of this study is to find a sweet spot, a point which has either a very low or cancelling 3rd and 2nd order response and to take advantage of the parallelism in improving the linearity.

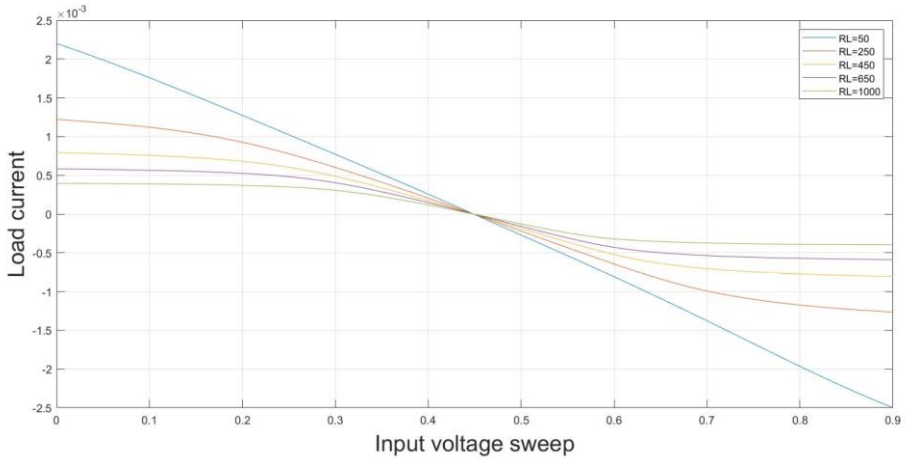

Figure 34: I-V curve of GM block at different output resistances.

Here the high value of the RL clearly compresses the output much sooner while with the low RL resistance value (the low RL load keeps the output voltage in the linear range) The GM block really behaves like a current output.

4.2.5 Varying output voltage at Rload = 50 Ω

As mentioned before in this part we are going to sweep the input voltage, steps up the output voltage from 0.3V to 0.7V and keep the load resistance at 50 Ω. We will study 3 cases when the output voltage is 0.3V, 0.4V and 0.6V.

The polynomial model is built for the load current as a function of the input voltage from dc term up to the third order coefficient. That was done by sweeping the bias point and at each point build the polynomial model of the I-V curve for +-50 mV from that bias point. The fitted model is recorded for each bias point, and eventually the polynomial coefficients are plotted as functions of the input bias.

4.2.5.1 case1 output voltage = 0.3V

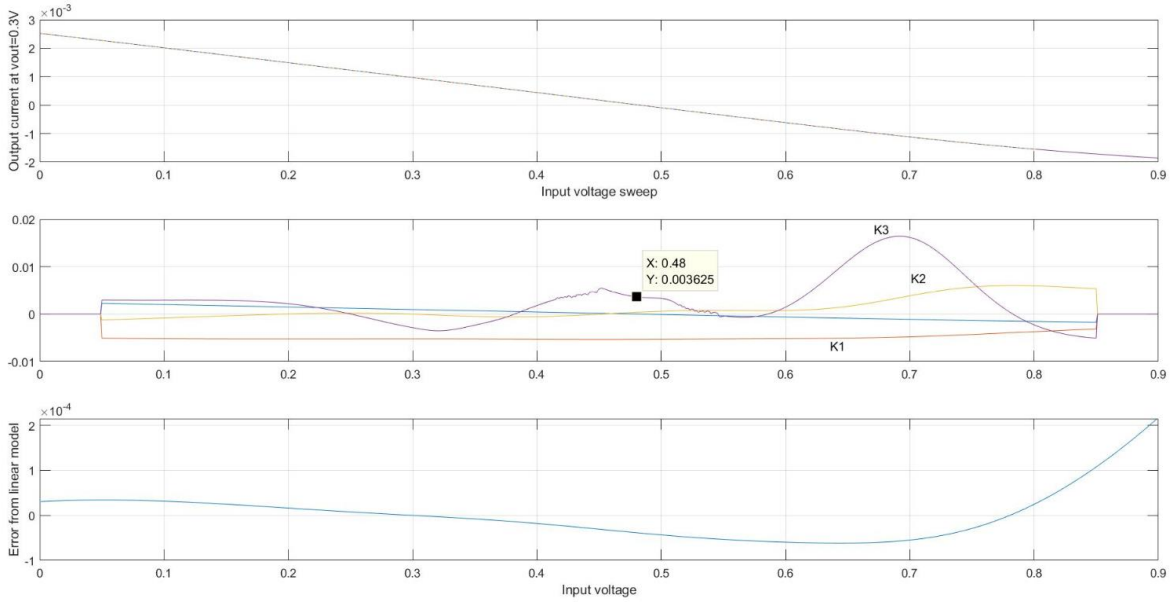

Figure 35: I-V curve, coefficients and error at case 1.

In each case, the I-V curve (output current, input voltage), polynomial coefficients (K1 first order, K2 second order and K3 third order) and the Error function (difference between the I-V curve and the linear model) are plotted.

Then the third order intermodulation distortion is calculated at the operating point and in the worst case (worst case is going to be calculated if the peak of the third coefficient curve is corresponding to an input voltage which will keep both the NMOS and PMOS transistor at saturation). The third order intermodulation is calculated according to equation (21).

Table 2: Response of case 1 at operating voltage.

Value of the Input voltage	**Response**
At the operating point (Vin = 0.48V)	Fund response = K1 A = (0.005326) (0.05) = -71.49 dB20.
	Third Order response = $\frac{3}{4} K3\ A^3 = (\frac{3}{4})$ (0.003625) $(0.05)^3$ = -129.37 dB20
	IM3 = $\frac{3}{4}\frac{K3}{K1} A^2$ = -57.8 dBc

From Figure 35, we can notice that there are points at which K3 = 0 and K2 = 0 which are sweet spots that we are interested in. For example, at input voltage = 0.545V, K3 is equal to zero and at input voltage = 0.45V, K2 is equal to zero. We can also notice that at certain input voltage K3 value is negative. For example, at input voltage = 0.35V, K3 equals -0.002335. This would be helpful spot that cancels the 3rd order coefficient if the other parallel LNA has an operating point that introduce positive third order coefficient. That will generate some IM3 cancelation.

4.2.5.2 case2 output voltage = 0.4V

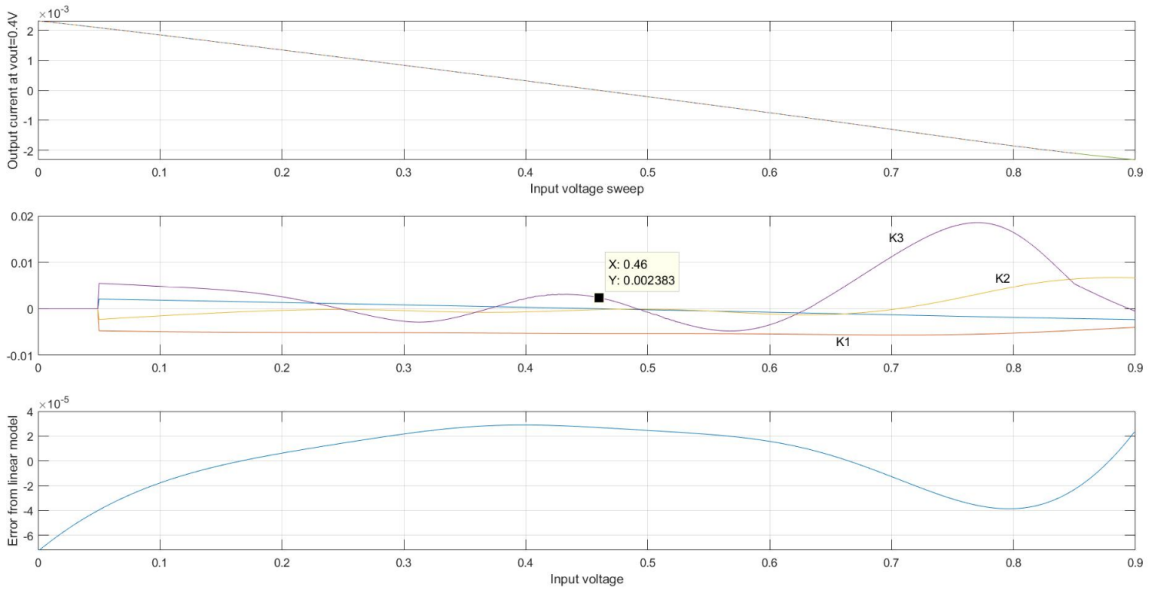

Figure 36: I-V curve, coefficients and error at case 2.

Table 3: Response of case 2 at operating voltage.

Value of the Input voltage	**Response**
At the operating point (Vin = 0.46V)	Fund response = K1 A = (0.005319) (0.05) = -65.48 dB20.
	Third Order response = $\frac{3}{4} K3\ A^3 = (\frac{3}{4})$ (0.002383) $(0.05)^3$ = -114.96 dB20
	IM3 = $\frac{3}{4}\frac{K3}{K1} A^2$ = -49.5 dBc

As a case of study, we will assume that the output voltage of the LNA is 0.3V. If we choose the input voltage to be 0.35V as an operating point. From Figure 37, K3 is equal to -0.002335

at this input voltage. If a parallel LNA has an output voltage of 0.4V, K3 value is 0.002397. That would introduce rather good cancellation as the resulting K3 is 0.000062. The final IM3 will be shown in Table 3.

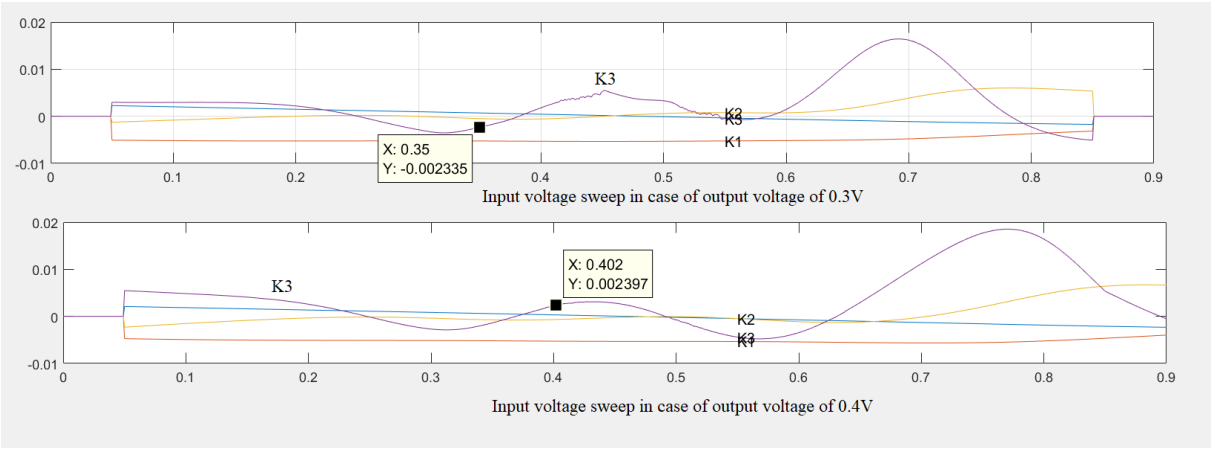

Figure 37: Studying of parallelism coeffiecients

Table 4: Response taking in account the parallelism.

Value of the offset voltages	**Response**
LNA 1 has output voltage of 0.3V and the other parallel LNA has output voltage 0.4V	Fund response = K1 A = (0.010645) (0.05) = -65.47 dB20.
	Third Order response = $\frac{3}{4} K3\ A^3 = (\frac{3}{4})$ (0.000062) $(0.05)^3$ = -164.7 dB20
	IM3 = $\frac{3}{4}\frac{K3}{K1} A^2$ = -99.24 dBc

As can be noticed that an improvement of almost 50 dB can happen in the value of the IM3 and this clearly improves the linearity. In practise much cancellation would require very stable conditions and biasing, and the practical cancellation continuous timing is often 20 dB.

It's important to remember that we have to choose an input voltage that will keep the NMOS and PMOS transistors at saturation and this will happen at a range of input between (0.35V to 0.55V).

4.2.5.3 case3 output voltage = 0.6V

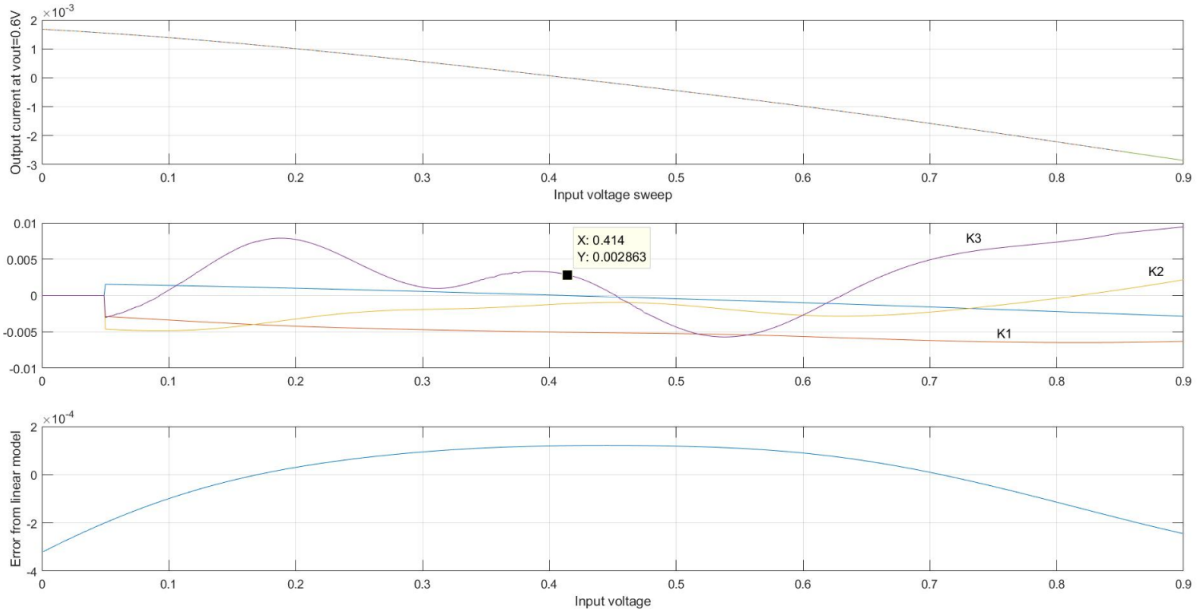

Figure 38: I-V curve, coefficients and error at case 3.

Table 5: Response of case 3 at operating voltage.

Value of the Input voltage	**Response**
At the operating point (Vin = 0.414V)	Fund response = K1 A = (0.005063) (0.05) = -71.932 dB20.
	Third Order response = $\frac{3}{4} K3\ A^3 = (\frac{3}{4})$ (0.002863) $(0.05)^3$ = -131.4 dB20
	IM3 = $\frac{3}{4}\frac{K3}{K1} A^2$ = -59.49 dBc

A point where K3≈0 can be found from Figure 38 at an input voltage of 0.452. At this point the IM3 = -92.1 dBc. So we could have a 30 dB improvement in the linearity at this point.

The worst-case scenarios are not calculated at all the previous cases as the peak of the third order coefficient curve happens at an input voltage which bring the PMOS transistor out of saturation.

It is worth mentioning that a normalization for the input signal was done to make sure that the convergence of the polynomial model is done properly.

All the previous results show that the GM block is quite linear with different values of the output voltage.

4.2.6 Varying output resistance at Vout = 0.45V

In this case the output voltage (load voltage) is kept at 0.45V and the output resistance is varied (we vary the input voltage from 0V to 0.9V and steps up the output resistance from 50Ω to 250Ω). We will study 2 different cases when Rout is equal to 50Ω and 250Ω.

4.2.6.1 case1 output resistance = 50Ω

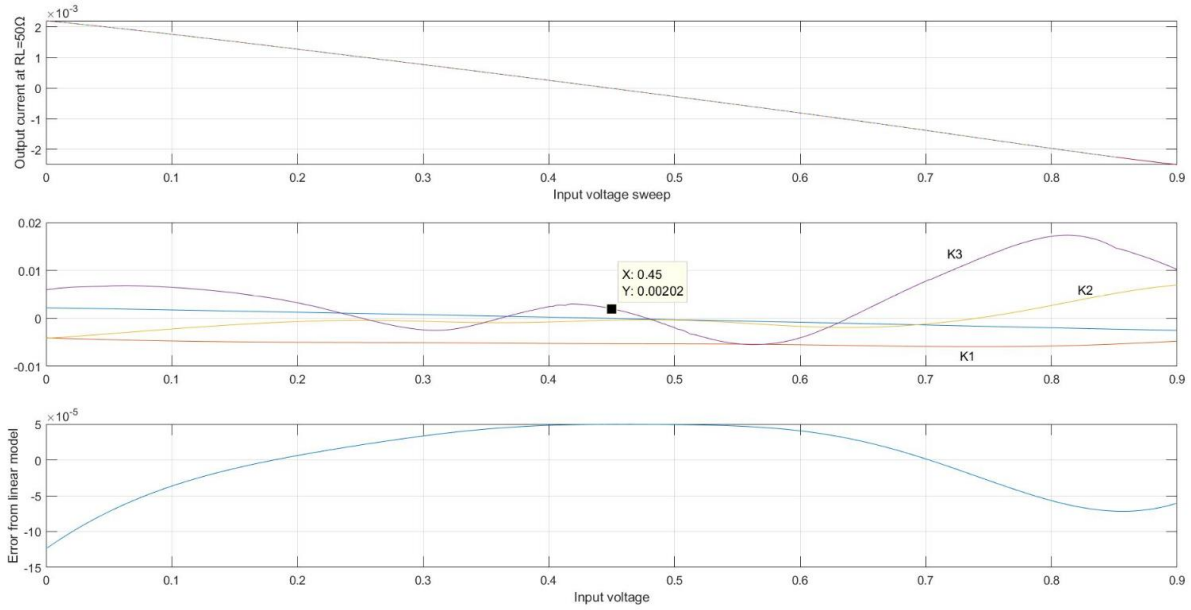

Figure 39: I-V curve, coefficients and error at case 1.

Table 6: Response of case 1 at operating voltage.

Value of the Input voltage	**Response**
At the operating point (Vin = 0.45V)	Fund response = K1 A = (0.005285) (0.05) = -71.559 dB20.
	Third Order response = $\frac{3}{4} K3\ A^3 = (\frac{3}{4})$ (0.00202) $(0.05)^3$ = -134.45 dB20
	IM3 = $\frac{3}{4}\frac{K3}{K1} A^2$ = -62.89 dBc

A point where K3≈0 can be found from Figure 39 at an input voltage of 0.478. At this point the IM3 = -95.2 dBc. So, we could have a 30 dB improvement in the linearity at this point

4.2.6.2 case2 output resistance = 250Ω

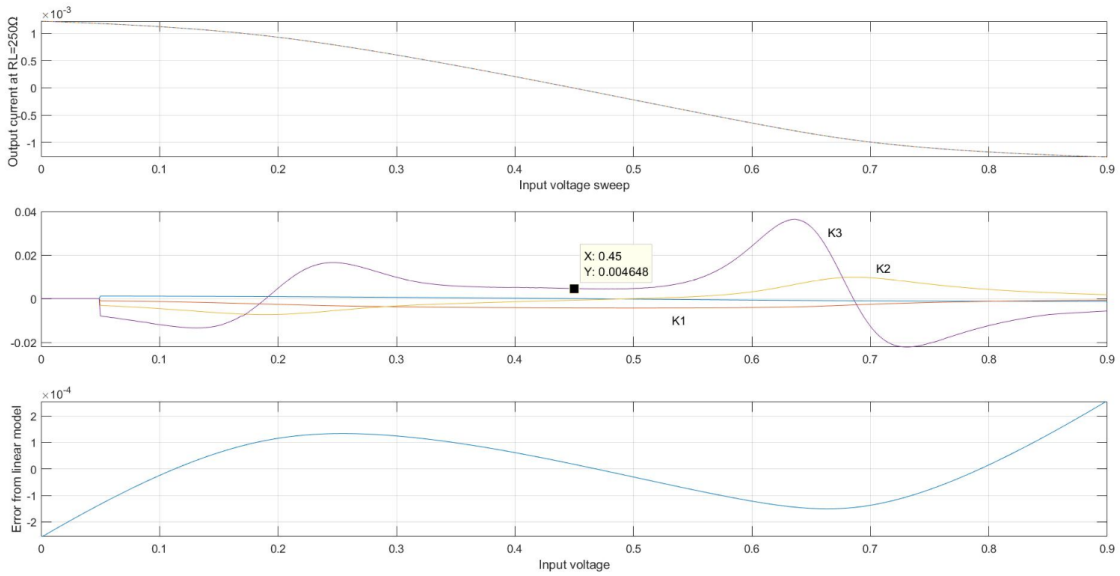

Figure 40: I-V curve, coefficients and error at case 2.

Table 7: Response of case 2 at operating voltage and the worst case.

Value of the Input voltage	**Response**
At the operating point (Vin = 0.45V)	Fund response = K1 A = (0.0042) (0.05) = -73.5 dB20.
	Third Order response = $\frac{3}{4} K3\ A^3 = (\frac{3}{4})$ (0.004648) $(0.05)^3$ = -127.2 dB20
	IM3 = $\frac{3}{4}\frac{K3}{K1} A^2$ = -53.7 dB
Worst case scenario (Vin=0.55V)	Fund response = K1 A = (0.0042) (0.05) = -73.5 dB20.
	Third Order response = $\frac{3}{4} K3\ A^3 = (\frac{3}{4})$ (0.008415) $(0.05)^3$ = -122.05 dB20
	IM3 = $\frac{3}{4}\frac{K3}{K1} A^2$ = -48.55 dB

The previous results show that the distortion increases as the output resistance increases. This was expected as increasing the output resistance will increase the voltage gain and hence the output voltage from the GM block will saturate sooner.

As the value of the output resistance increases the nonlinearity of the block increases and it's hard to have an input voltage that is corresponding to K3 = 0 (or sign reversal). Hence it is difficult to do some cancellations of the distortion.

It is important to remember that the use of the GM block is to convert the input voltage to output current and since the GM value of the GM block is 5mS and the GM block is followed by a passive mixer which add more losses a question may arise to the reader concerning the total gain per branch. The gain is going to recover by means of two factors, the first one from the addition from different slot and from the transimpedance amplifier which has a transimpedance gain of approximately 70 dB.

5 ANALYSIS OF THE MIXER BLOCK

Passive mixers have become an essential component in the state of the art wireless transceivers. They have replaced active mixers in most implementations due to their superior linearity, good voltage headroom, and low power consumption and 1/f noise.

The primary sources of nonlinearity in a passive CMOS mixer driven by square wave LO are: nonzero rise and fall time of the LO, nonlinear Cgs and Cgd, nonlinear relationship between the VDS and ID. At lower RF frequencies a square wave (LO) can faithfully be achieved in an IC environment. Hence, the contribution from the finite rise and fall time and nonlinear capacitance can be neglected at those frequencies.

Device mismatches in the differential structure may cause some nonlinearities. For example, for the ideal differential pair, the even order distortion will appear as a common mode signal and will be rejected in the differential operation but the device mismatches and layout effects will make the differential paths unequal and some even order distortion will appear at the output. The threshold voltage mismatch among the switches will cause the on-state conductance to vary among the switches.

5.1 Passive mixer conversion gain

The single ended passive mixers can be realized with a simple NMOS device as shown in Figure 41.

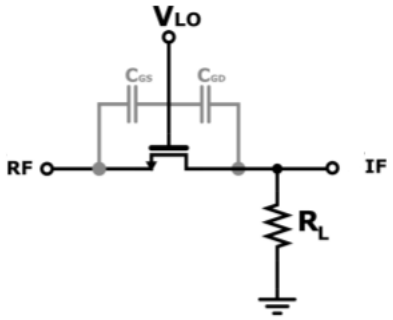

Figure 41: Schematic of single ended passive mixer.

Passive mixer's converting action is characterized by conversion loss. The passive mixer is considered as voltage-controlled resistor varying between on (Ron) and off (Roff ~infinity) with a square wave clock with some duty cycle D of 50% at this case.

Two single balanced mixers can be connected such that the output LO feedthrough is cancelled out. This topology is shown in Figure 42 and is called double balanced mixer.

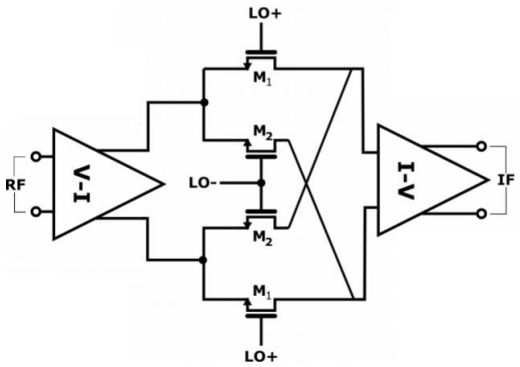

Figure 42: Schematic diagram for double balanced mixer and its gain

In order to see the effect of the duty cycle on the current cumulating mixer. We modelled the GM stage as a current source with a certain load impedance and a quadrature mixer with four outputs representing I+,I-,Q+,Q- is used. The transimpedance amplifier is modelled as a simple low impedance resistor.

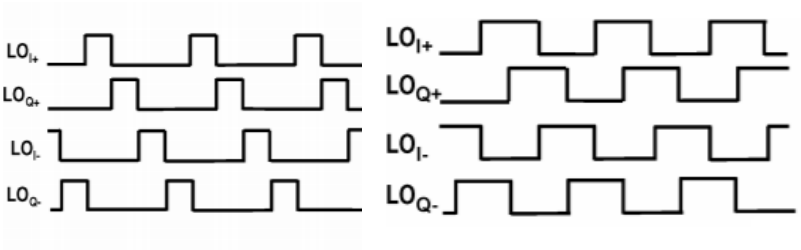

Figure 43: Ideal 25% and 50% duty cycle LO signal respectively.

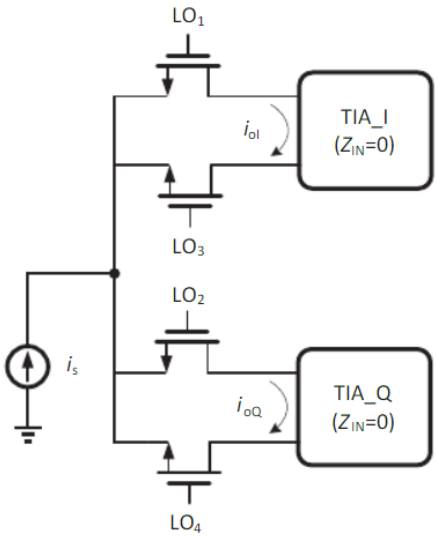

Figure 44: Quadrature mixer model.

The aim is to vary the duty cycle and see its effect on the conversion gain. We can expect that in the case of less than 25% duty cycle, there will be some period at which all the switches are off which reduces the gain. For the case of more than 25% duty cycle, there will be some cases where 2 switches are on, this leads to the splitting of the RF current between two branches

which means that the differential output will drop dramatically. A graph for the conversion gain can be shown in Figure 45.

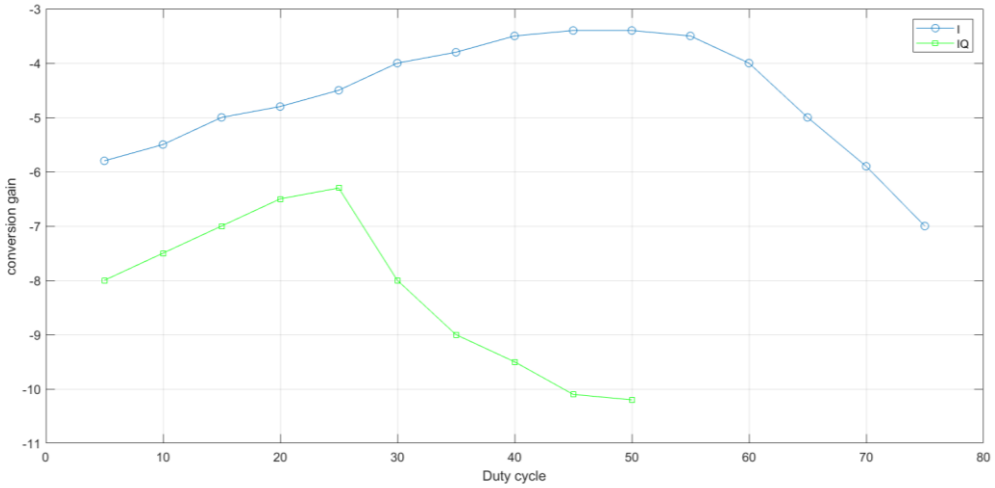

Figure 45: Conversion gain for different duty cycles.

5.2 Passive mixer non reverse isolation property

The passive mixers have no reverse isolation as they are intrinsically bidirectional which results in the interaction between the inputs and the outputs of the passive mixer. so, as a conclusion the input resistance of the passive mixer is dependent on the baseband impedance which is an RC circuit. The input impedance of the passive mixer exhibits bandpass filtering centered at the LO frequency. This was initially introduced by [12]. The work is even extended to become the passive first mixer. The dependency of the input impedance of the mixer on the RC baseband impedance was used to match the input impedance to 50Ω and eliminate the LNA. The linearity of the passive mixer first architecture is high, but this comes at the cost of the noise figure which is high in this receiver architecture.

Another important observation to note is that the voltage swing on the mixer RF node is a combination of the translated baseband voltage swing and the RF signal itself. In case of the undesired received signal, the current in beamforming receiver will be added destructively (out of phase currents) which leads to low voltage swing at both the output of the LNA and the baseband. This leads to improvement in the linearity (IIP3 value).

The input impedance for the passive mixer loaded with the transimpedance amplifier can be shown in Figure 46. Assuming that the direct conversion receiver has LO frequency of 2GHz.

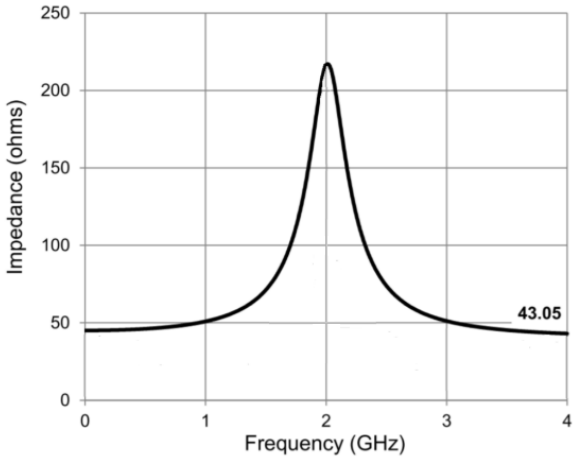

Figure 46: Input impedance of double balanced passive mixer.

The schematic used for Figure 46 is similar to what is shown in Figure 42. The input impedance is measured from the RF side. The TIA (I-V) appears as ZT/(1-Au), where Au is negative and Zt is a parallel combination of R and C.

5.3 Passive mixer discontinuity problem

The NMOS transistor in the passive mixer is biased in deep triode with the DC voltage VDS=0. The shape of the I-V curve of BSIM3/BSIM4 model at VDS = 0 bias deviates from measured results due to the discontinuities in the higher order derivatives of the drain current and terminal charges. The models are typically tested for Gummel symmetry [11] where equal and opposite voltages are applied at the source and the drain terminals of the MOSFET and the drain current is measured.

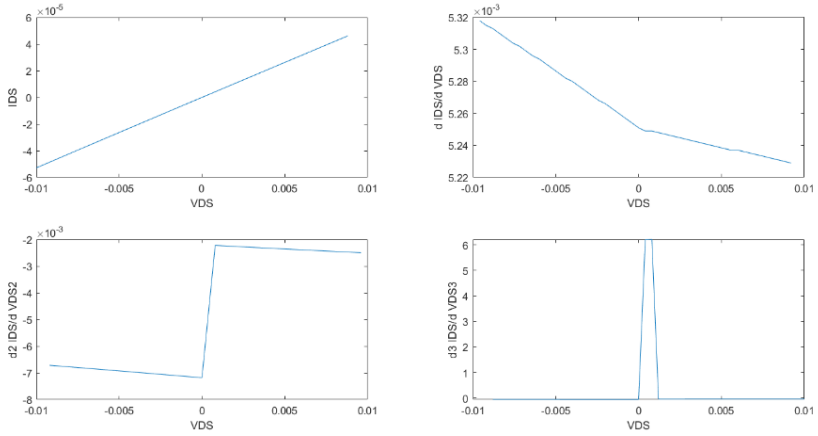

Figure 47: IDS and first three derivatives with respect to VDS.

Figure 47 shows the IDS vs VDS and the first three derivatives vs VDS. This is done for the 45 nm technology. This illustrates the anomalous third order distortion slope of 2:1 instead of 3:1 shown in Figure 48. The PSP [11]

model uses a single equation to define the drain current across all the biasing conditions which yields in a continuous first and higher order derivatives.

A comparison between The IIP3 value with the BSIM3 and the PSP setups for the passive single ended mixer is shown in Figure 48.

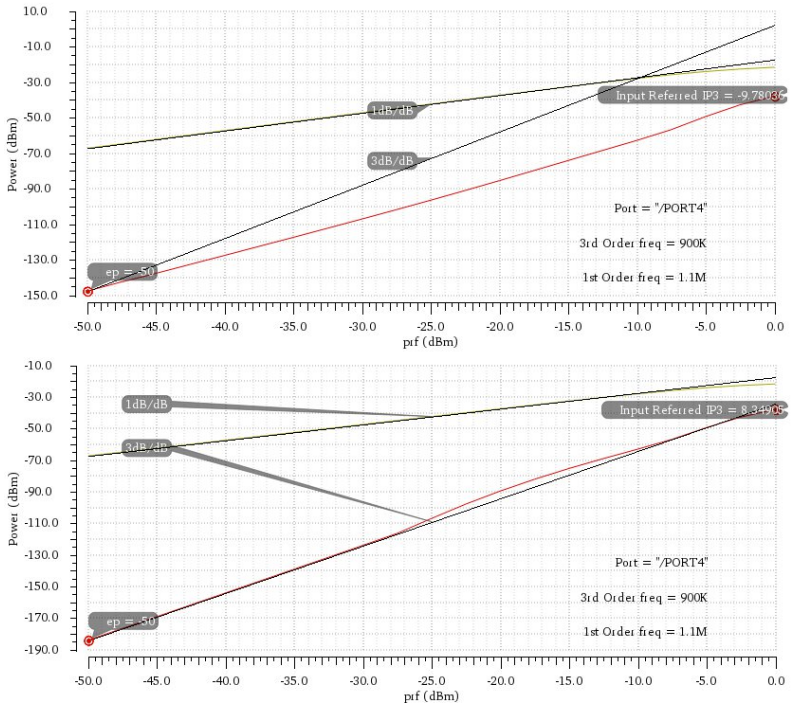

Figure 48: IIP3 values from the BSIM and PSP models.

In Figure 48, the upper plot is the BSIM4 model while the down plot is the PSP model results. The IIP3 value in case of the BSIM3/4 models is -9.7dB which is not a realistic value while the IIP3 in case of the PSP model is 8.34 dB which is more realistic value. The two tones frequencies used in the simulation are 3.001 GHz and 3.0011 GHz while LO signal frequency is 3 GHz. The choice of the two tones blocker should be on such a way that their third order intermodulation product is falling within the signal band in the baseband.

5.4 Passive mixer IIP3 value

The linearity of the double balanced mixer can be studied by measuring the IIP3 as shown in Figure 49. As can be seen in section 5.3, the BSIM3/4 is not giving realistic value so it is recommended to use the PSP model as the transistors are biased in deep triode with DC drain to source voltage equal to zero.

For the single ended passive mixer, the IIP3 is shown in Figure 48. The IIP3 value of the PSP model is 8.34 dB.

For the differential passive mixer shown in Figure 42, the IIP3 value is shown in Figure 49. The IIP3 value of the PSP model is 14.06 dB. This concludes that the differential passive mixer is more linear than the single ended one.

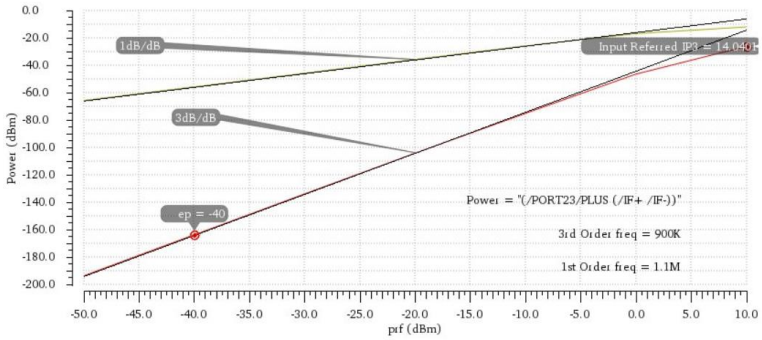

Figure 49: IIP3 of the differential passive mixer.

The two tones frequencies are 4.001 GHz and 4.0011 GHz while LO signal frequency is 4 GHz. The two down converted signals are at 1MHz and 1.1GHz and the third order distortion will appear at 0.9MHz.

5.5 Nonlinearity analysis

In the receiver design, the GM stage is DC coupled to the mixer stage that was done to avoid large coupling capacitance at each slice and to avoid operating point mismatch, a CMFB circuit is connected to the output of the GM stage to set the common mode output voltage. Then the passive mixer current drives the transimpedance amplifier which provide the output baseband voltage. Typically, the common mode feedback loop of the TIA provides the DC bias to the output terminal of the mixer. The transistors of the mixer are biased in the deep triode region as VDS is very small ≈ 0. So that there is no DC current passing the transistors.

At the beginning, we studied the effect of the parallelism in improving the linearity of the mixer. The following schematic is built.

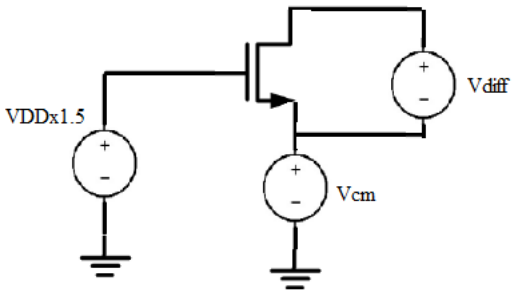

Figure 50: Schematic used for the mixer linearity analysis.

A polynomial model for the IDS vs Vdiff is built for different voltages at a given common mode level. Then the first, second and third order coefficients are drawn versus the differential voltage.

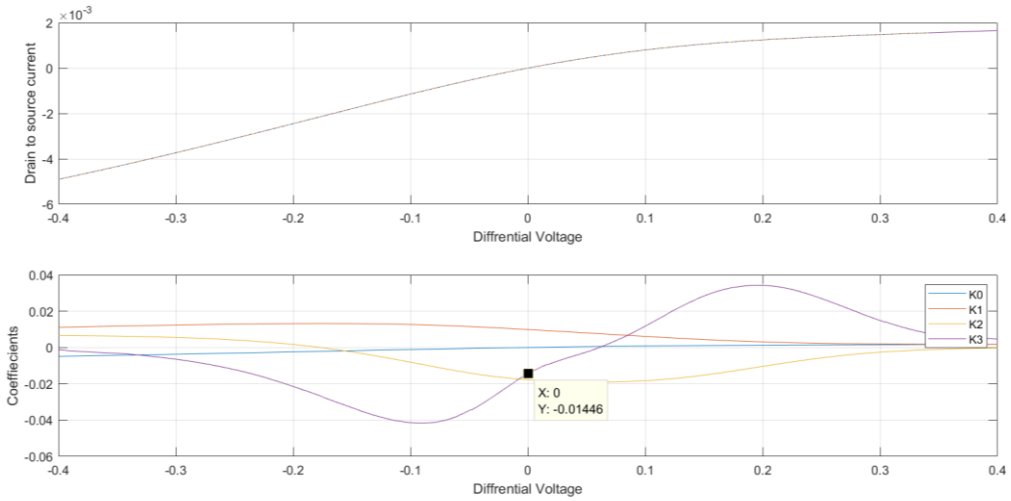

Figure 51: Coefficients in case of Vcm=0.1V

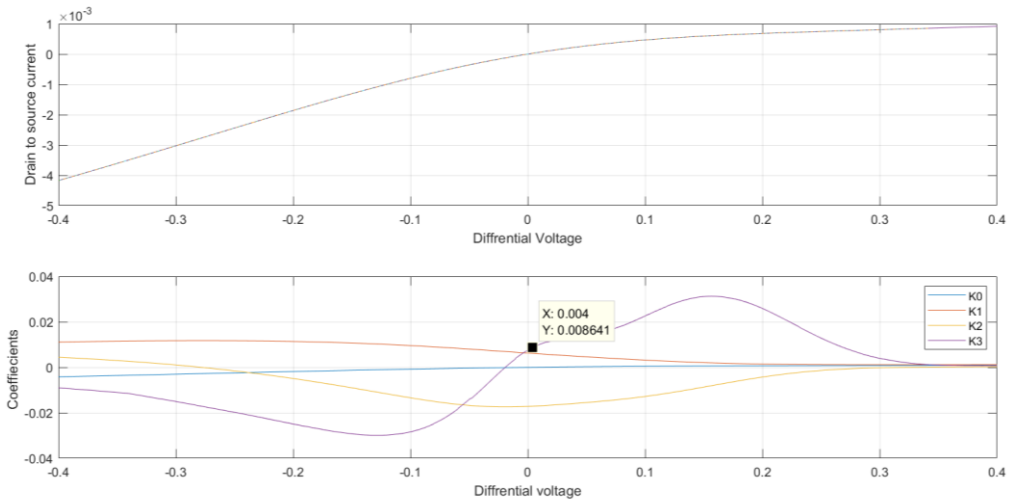

Figure 52: Coefficients in case of Vcm=0.2V

From Figure 51 and Figure 52, we notice that at two different common mode voltages the values the third order coefficients show two different signs. This could produce some cancellations in the combined parallel structure as shown in the following table.

Table 7: Third order intermodulation distortion taking advantage of parallelism.

Operating point	**Response**
At Point VDS=0	Fund response = K1 A = (0.016139) (0.05) = -81.86 dB20.
	Third Order response = $\frac{3}{4} K3\ A^3 = (\frac{3}{4})$ (0.005817) $(0.05)^3$ = -125.26 dB20
	IM3 = $\frac{3}{4}\frac{K3}{K1} A^2$ = -43.4 dB

From the previous results, we can notice that the parallelism could improve the linearity by approximately 10 dBs, noting that the IM3 value without parallelism is -35.2 dB.

It is important to note that the previous analysis needed to be done using the PSP model as the BSIM3/4 produce huge third order distortion at the point Vds=0. In the DC-connected case

Vcm needs to raise close to VDD, which makes Vgs-Vt. The gate swing could increase but there is a risk of oxide breakdown. That is handled by the fact that Vcm does not go down to zero.

The transistor can be modelled as a linear transconductance [11]. While the GM stage can be modelled as a current source with a shunt impedance Zs and the load impedance of the mixer which is the input impedance of the transimpedance amplifier is modelled as ZL. This can be shown in Figure 53.

The 2D modelling for the i_{DS} is as in the following equation.

$$\begin{aligned} i_{\mathrm{DS}} = {} & K_{100}\, v_{\mathrm{gs}} + K_{200}\, {v_{\mathrm{gs}}}^2 + K_{300}\, {v_{\mathrm{gs}}}^3 \\ & + K_{010}\, v_{\mathrm{ds}} + K_{020}\, {v_{\mathrm{ds}}}^2 + K_{030}\, {v_{\mathrm{ds}}}^3 \\ & + K_{110}\, v_{\mathrm{gs}}\, v_{\mathrm{ds}} + K_{210}\, {v_{\mathrm{gs}}}^2\, v_{\mathrm{ds}} + K_{120}\, v_{\mathrm{gs}}\, {v_{\mathrm{ds}}}^2 \end{aligned} \tag{51}$$

An alternative approach to fit the polynomial device model is used in [22], which performs the fit in the frequency domain. The technique is based on fitting the polynomial model using the convolved large-signal spectra of the controlling voltages and the current spectrum of the corresponding. This paper shows that it is possible to use the fitted coefficients and the convolved spectra of the controlling voltages to perform a simplified Volterra analysis. In general, the contributions of the selected distortion current can be calculated by multiplying the fitted coefficients with the selected tone phasor of the corresponding higher order voltage spectra.

$$\begin{aligned} I_{\mathrm{DS}}(f_{\mathrm{IM3}}) = {} & K_{10}\, V_{10}(f_{\mathrm{IM3}}) + 2K_{20}\, V_{\mathrm{ENV}}(f_{\mathrm{IM3}}) \\ & + 2K_{20}\, V_{H2}(f_{\mathrm{IM3}}) + K_{30}\, V_{30}(f_{\mathrm{IM3}}) \\ & + K_{10}\, V_{10}(f_{\mathrm{IM3}}) + K_{02}\, V_{02}(f_{\mathrm{IM3}}) \\ & + K_{03}\, V_{03}(f_{\mathrm{IM3}}) + K_{11}\, V_{11}(f_{\mathrm{IM3}}) \\ & + K_{21}\, V_{21}(f_{\mathrm{IM3}}) + K_{12}\, V_{12}(f_{\mathrm{IM3}}) \end{aligned} \tag{52}$$

where, $V_{10}(f)$ and $V_{01}(f)$ is the measured $V_{GS}(f)$ and $V_{DS}(f)$ voltage spectra, respectively. The higher order spectra that are marked as $V_{nm}(f)$ corresponding to a nonlinear term $V_{\mathrm{GS}}(t)^n . V_{\mathrm{DS}}(t)^m$. As an example, $V_{30}(f)$ is obtained from $V_{\mathrm{GS}}(f) \otimes V_{\mathrm{GS}}(f) \otimes V_{\mathrm{GS}}(f)$, while $V_{21}(f)$ is obtained from $V_{\mathrm{GS}}(f) \otimes V_{\mathrm{GS}}(f) \otimes V_{\mathrm{DS}}(f)$ and so on. V_{ENV} is the second order distortion at the baseband. V_{H2} is second harmonic voltage which can mix further to third order intermodulation distortion.

Since the controlling voltages in passive mixer are corelated, there might be difficulties in fitting.

From Figure 53, we have two KCL equations.

$$\frac{v_1 - v_2}{Ron} + \frac{v_1}{Z_{\mathrm{s}}(w)} = i_{\mathrm{rf}} - i_{\mathrm{NL}} \tag{53}$$

$$\frac{v_2 - v_1}{Ron} + \frac{v_2}{Z_{\mathrm{L}}(w)} = i_{\mathrm{NL}} \tag{54}$$

From these two equations, we can get the linear voltages (v_1, v_2) when $i_{\mathrm{NL}} = 0$.

$$v_1 = \frac{(Z_{\mathrm{L}}(w) + Ron) Z_{\mathrm{s}}(w)}{Z_{\mathrm{s}}(w) + Z_{\mathrm{L}}(w) + Ron}\, i_{\mathrm{RF}} \tag{55}$$

$$v_2 = \frac{Z_s(w)Z_L(w)}{Z_s(w) + Z_L(w) + Ron} i_{RF} \tag{56}$$

Then the distortion voltage can be calculated by the nonlinear current injection method. So, by substituting i_{RF}=0 in equations (53, 54).

$$v_{1NL} = \frac{Ron\ Z_s(w)}{Z_s(w) + Z_L(w) + Ron} i_{NL} \tag{57}$$

$$v_{2NL} = \frac{Ron\ Z_L(w)}{Z_s(w) + Z_L(w) + Ron} i_{NL} \tag{58}$$

where, v_{1NL} and v_{2NL} are the distortion voltages. Those distortion voltages could be due to the second or third order nonlinear currents, those nonlinear currents values can be derived as in equation (52). $i_{NL}(f_{IM3})$ is the time domain representation of $I_{DS}(f_{IM3})$.

In the current commutating passive mixer, typically $Z_s(w) \gg$ Ron and $Z_L(w)$ so that the voltages can be approximated to

$$v_1 = (Z_L(w) + Ron) i_{RF} \ \ \& \ \ v_2 = Z_L(w)\ i_{RF} \tag{59}$$

$$v_{1NL} = \ Ron\ i_{NL} \ \ \& \ \ v_{2NL} = \frac{Ron\ Z_L(w)}{Z_s(w)} i_{NL} \tag{60}$$

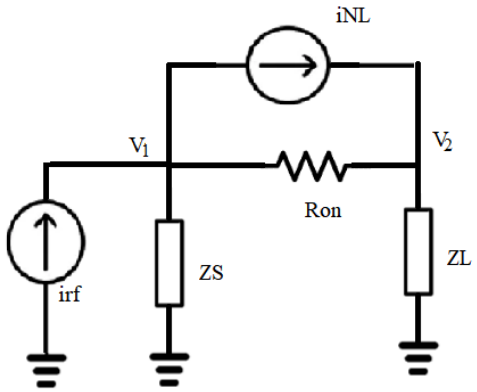

Figure 53: Modelling single ended passive mixer.

For the two tones input w_1, w_2, the IP2 refers to the input is

$$IIP2 = \frac{P_{out}(W_{LO} - W_1)}{P_{out}(W_1 - W_2)} P_{in}(W_1) = \left[\frac{v_2(W_{LO} - W_1)}{v_{2NL}(f_{IM2})}\right]^2 P_{in}(W_1) \tag{61}$$

Assuming 50Ω match at the LNA input, then $P_{in}(W_1)$ is calculated according to the following equation.

$$P_{in}(W_1) = \frac{{i_{RF}}^2}{50\ {g_{m,LNA}}^2} \tag{62}$$

Then substitute (59,60) in equation (61). The resulting equation

$$IIP2 = \left[\frac{Z_{\mathrm{L}}(W_{LO} - w_1)Z_{\mathrm{s}}(w_1 - w_2)}{Ron\, Z_{\mathrm{L}}(W_{LO} - (w_1 - w_2))} \frac{i_{\mathrm{rf}}}{i_{\mathrm{NL}}(f_{\mathrm{IM2}})}\right]^2 P_{in}(W_1) \tag{63}$$

As can be notice from equation (63) that for a high IIP2, $|Z_{\mathrm{s}}(w_1 - w_2)|$ need to be as large as possible. Physically, a low source impedance at $(w_1 - w_2)$ amplifies the IMD2 currents due to the mismatches in the mixer transistors or LO signals. In a typical receiver, the parasitic capacitances at the LNA–mixer interface can lower the input impedance [22].

Since the passive mixer is typically cascaded with a TIA, the mixer load impedance is low at dc, but increases rapidly with frequency as the open-loop TIA gain drops. Hence, the down converted jammers outside the desired signal band encounter a relatively high TIA input impedance.

The IP3 refers to the input can be calculated as in the following equation

$$IIP3 = \left[\frac{P_{out}(W_{LO} - W_1)}{P_{out}(W_{LO} - (2W_1 - W_2))}\right]^{0.5} P_{in}(W_1) \quad = \frac{v_2(W_{LO} - W_1)}{v_{2NL}(f_{\mathrm{IM3}})} P_{in}(W_1) \tag{64}$$

Then substitute (59,60) in equation (64). The resulting equation

$$IIP3 = \frac{Z_{\mathrm{L}}(W_{LO} - w_1)Z_{\mathrm{s}}(2w_1 - w_2)}{Ron\, Z_{\mathrm{L}}(W_{LO} - (2w_1 - w_2))} \frac{i_{\mathrm{rf}}}{i_{\mathrm{NL}}(f_{\mathrm{IM3}})} P_{in}(W_1) \tag{65}$$

As can be notice from the previous equation that for a high IIP3 $Z_{\mathrm{L}}(W_{LO} - (2w_1 - w_2))$ should be minimized. This term is corresponding to load impedance at high frequency, which is small due to the large filtering capacitor at the mixer output.

For the differential operation, the fundamental and third-order voltages will be doubled, while the second-order voltage will be cancelled, $i_{\mathrm{NL}}(f_{\mathrm{IM2}}) = 0$.

5.6 Mixer output common mode

MOSFET on resistance has the property that it increases as the drain to source voltage increases. This is shown in Figure 54. This causes the mixer to inject a negative common mode to the next block (Transimpedance amplifier).

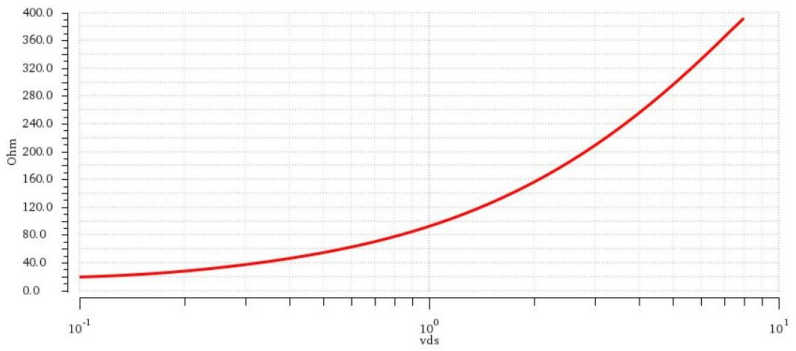

Figure 54: On resistance vs VDS of the used transistor.

In the double balanced mixer, positive and negative half of the RF signal is applied to the drains of the transistors M1 and M4 as shown in Figure 55. In this case the upper transistor will have high on resistance value while the down transistor at the same moment will have low on resistance value. This will generate output common mode voltage.

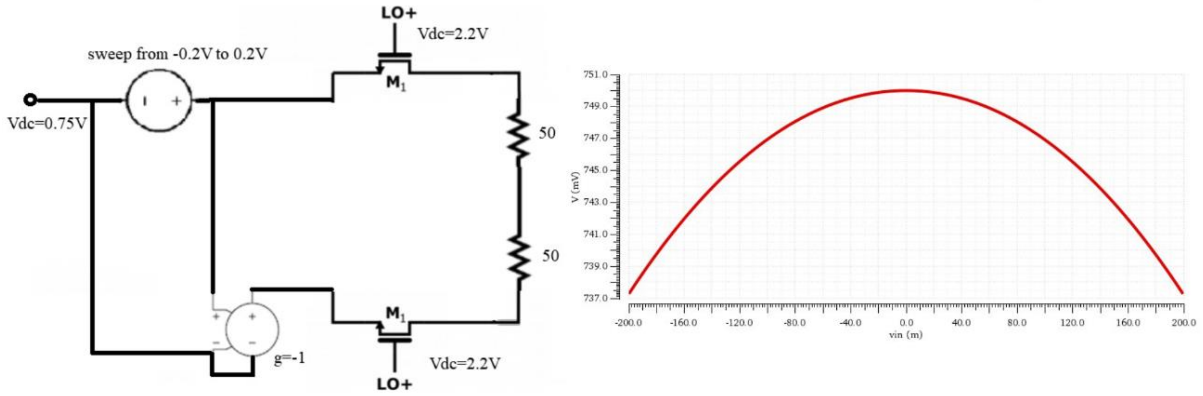

Figure 55: Schematic diagram for output common mode voltage.

In this simulation, a 400 mV differential input voltage sweep causes -13 mV common mode output voltage. Hence the transimpedance amplifier which is the following block needs to react with the continuously varying common mode level in its input and this may have some dynamic effects.

This happens in addition to the DC offset that occurs due to the leakage of the LO waveform to the input of the mixer. If the transistors are perfectly symmetric, the DC offset will vanish. but in practice, there is always mismatches between the devices. A rough rule of thumb is 10-20 mV at the output of the mixer.

6 DISCUSSION

This thesis discusses a typical modern receiver where a transconductance amplifier is used as an TLNA and provide input matching. The TLNA is driving a current mode passive mixer and finally a transimpedance amplifier.

Our main focus is to study the linearity of the both the TLNA and the passive mixer. The linearity is studied by building polynomial model of the I-V data and study the first, the second and third order coefficients change with the bias point. The results are showing very high linearity for the TLNA by properly choosing the correct bias point. We also show that by linearity can even improve more by taking advantage of the parallelism. For example, the linearity of the passive mixer can improve by 10 dBs and up to50 dBs for the TLNA.

As the passive mixer is working at VDS=0, it is important to know that the BSIM3/4 has discontinuities in the higher order derivatives of the drain current and terminal charges at this point. So, we recommend to use the PSP model which uses a single equation to define the drain current across all the biasing conditions which yields in a continuous first and higher order derivatives. As a conclusion the PSP model gives more reliable results for the IIP3 of the passive mixer than the BSIM3/4.

The passive mixer shows bidirectional property, where the input impedance of the passive mixer is dependent on the baseband impedance. This impedance shows a bandpass filtering centered around the LO frequency. Also, this bidirectional property causes the voltage swing on the mixer RF node is a combination of the upconverted baseband voltage swing and the RF signal itself.

The passive mixer injects negative common mode to the TIA (in 1.5V supply simulation bench 400 mV differential signal caused -13 mV common mode signal, or about -30 dB). Hence, the TIA needs to react with continuously varying cm level in its input and this may have some dynamic effects. This happens in addition to the DC offset that occurs due to the leakage of the LO waveform to the input of the mixer.

In studying the linearity of the GM stage, we had some concerns about the second order polynomial coefficient value (k2) in the case of biasing for a small value for the third order polynomial coefficient (k3). The IM3 non-linearity for the cascaded GM-mixer stage is either dominated by k3 or cascaded k2. In MOS devices it is often the latter. Also, in the single MOS device, Taylor series higher order coefficient is the derivative of the previous, hence if k3 is zero, k2 should be either in minimum or maximum. This seems not to be the series case in the inverter GM structure due to the multiple minimas both K3 and K2 have (both can be chosen to be small). This probably comes from the NMOS/PMOS pair cancellation (combined effect of the two non-linearities).

For the cascaded GM stage and mixer, the IM3 value is calculated through two different ways in order to know the dominating source of non-linearity. The first one takes in to account the value of k3 only and the other one takes into account the cascaded 2^{nd} order harmonics. The values of IM3 are -60dBc and -67dBc respectively. This is in the case of the 45nm technology. The previous results show that the cascaded 2^{nd} order non-linearity will not affect much the value of IM3.

Most of the linearity analysis were made based on DC I-V curves of the blocks. As a next step of research, also the dynamic effects due to nonlinear capacitances and LO feedthroughs should be studied. Also, the effect of the common-mode control bandwidth would be the next thing to be done in further study.

7 SUMMARY

This thesis discusses the phased array receivers which are widely used nowadays in the 5th mobile generation. It starts with introducing some of the implemented receivers for example, the cartesian combing receiver, the constant GM beamformer receiver and finally the wideband scalable beamforming receiver. The difference between the implementation of those receivers is discussed.

In chapter 3, some of the basic concepts for studying the linearity of the receiver are introduced for example IIP2, IIP3 and compression point. we also introduce some of the basic series used in the linearity analysis for example, Volterra, polynomial and Taylor series. A comparison of the accuracy of each series was discussed and the ways of extracting the IM2 ,IM3, IIP3, etc. were also introduced for each of the previously stated series.

This thesis is analysing one slice from the wideband scalable receiver introduced by R.Akbar [5], studying its parameters and introduce new ways for improving the linearity by taking advantage of the parallelism. This receiver depends on the idea of both the cartesian combining introduced by J.Paramesh [2] and the constant GM vector modulator introduced by M.C.M.Soer [4]. The main idea of this receiver is to introduce the scalable solution in the cases when we have large number of antennas, for example 64. Our main concern in this receiver is the IF module band which is consists of the pseudo differential inverter based transconductance low noise amplifier, quadrature passive mixer and phase switches. Instead of exploiting charge sharing on a capacitor, that results in averaging, cartesian combining is implemented by true current summing into a virtual ground node provided by a transimpedance amplifier. This provides more gain and bandwidth.

In chapter 4, we introduce the design of the GM stage, provide some notes about the TLNA noise figure, input and output matching. Then the linearity of the GM stage was studied by building the polynomial model of the I-V curve and studying the first, second and third order coefficients. This is done for two different cases, the first one when we have output resistance of 50 Ω and varying the output voltage (we vary the input voltage from 0V to 0.9V and steps up the output voltage from 0.3V to 0.7V and fix the load resistance to 50 Ω). The aim is to know if there is a possibility of introducing minor offset in the output operating point of the parallel blocks so that the 3rd order coefficients would have opposite signs. This would then cause some cancellation of distortion in the combined output. We found that by taking advantage of parallelism, the linearity could increase by 50 dB. The other finding is at some bias point, the third order coefficient is zero (sweet spots) which could improve the linearity by 30 dB. The polynomial model is built for the load current as a function of the input voltage from dc term up to the third order coefficient. That was done by sweeping the bias point and at each point build the polynomial model of the I-V curve for +-50 mV from that bias point. At each time record the coefficients and finally we plot them against the input voltage sweep.

In chapter 5, The passive mixer parameters (gain, input impedance and linearity) are studied. We found that the gain of the differential mixer is -4dB, the IIP3 is 14dBm. We also introduce Polynomial series analysis for the linearity analysis of the passive mixer and find an expression for the IIP3 which gives us more intuitive understanding and provide us with the parameters needed to be improved for a better IIP3 value. Another important finding is that parallelism could improve linearity by 10 dB.

We also find that The BSIM3/BSIM4 model at VDS = 0 bias deviate from measured results due to the discontinuities in the higher order derivatives of the drain current and terminal charges so using these models to obtain the IIP3 will give non-realistic results. Another important finding is that the passive mixers have no reverse isolation as they are intrinsically

bidirectional which results in the interaction between the inputs and the outputs of the passive mixer. So, as a conclusion the input resistance of the passive mixer is dependent on the baseband impedance which is an RC circuit. The input impedance of the passive mixer exhibits bandpass filtering centered at the LO frequency.

We also found that the mixer to inject negative common mode to the TIA (in 1.5V supply simulation bench 400 mV differential caused -13 mV common mode, or about -30 dB). Hence, the TIA needs to react with continuously varying cm level in its input and this may have some dynamic effects. This happens in addition to the DC offset that occurs due to the leakage of the LO waveform to the input of the mixer.

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